17062083 Announcing Si8920 Revision B with Datasheet Revision 1.0

PCN Issue Date: 6/20/2017 **Effective Date:** 9/25/2017

PCN Type: Datasheet; Product Revision

Description of Change

Silicon Labs is pleased to announce an enhancement to the robustness of the OTP (One-Time Programming) circuit utilized in this product. In addition, calibration registers at production test have been changed to address a possibly larger than expected gain error issue. Datasheet revision 1.0 has been released with significantly improved non-linearity and offset specifications as well as increased IVDDB due to the calibration register change.

Reason for Change

The physical layout of the Si8920 OTP circuit was changed to improve robustness and calibration registers at production test were changed to address a possibly larger than expected gain error issue.

Impact on Form, Fit, Function, Quality, Reliability

There is no impact on form, fit, or function with revision B product. The change in calibration results in improved linearity and offset specifications and an increase in IVDDB current which is reflected in the 1.0 revision datasheet. All quality and reliability checks have been done and show no impact with these changes other than the specifications listed.

Product Identification

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Existing Part #
Si8920AC-IP
Si8920AC-IPR
Si8920BC-IP
Si8920BC-IPR
Si8920AD-IS
Si8920AD-ISR
Si8920BD-IS
Si8920BD-ISR
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Last Date of Unchanged Product: 9/25/2017

Qualification Samples

Samples available upon request.

Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

In some cases rejection of a change notice may impact Silicon Labs product pricing, delivery, quality, or reliability.

Customer Early Acceptance Sign Off

Customers may approve early PCN acceptance by completing the information below:

Early Acceptance:

Date: _____

Name:_____

Company:_____

Email your early Acceptance approval to: PCNEarlyAcceptance@silabs.com

User Registration

Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, “how-to” and design documents, product change notices (PCN) and other valuable content available only to registered users. **http://www.silabs.com/profile**

Qualification Data

See Qualification Report in Appendix below.

Si892x AEC-Q100 Qualification Report

W7101F1 - Product Qualification Report Record Rev. I

Part Rev A, Vanguard Fabrication, UTL Assembly except as noted							
Test Name	**Test Condition**	**Qualification**	**Lot ID or Start**	**Fail/Pass or End**	**Notes**	**Summary**	**Status**
Test Group A – Accelerated Environment Stress Tests - 8-Pin PDIP							
HAST	JA110		Q033698	0/80	1, 2		
	130°C, 85%RH	3 lots, N=>77	Q033744	0/80	1, 2	3 lots	Pass
	Vcc=5.5V, 96 hours		Q033746	0/80	1, 2	0/240	
Temp Cycle	JA104		Q033120	0/80	1, 2		
	Cond C: -65°C to 150°C	3 lots, N=>77	Q033743	0/80	1, 2	3 lots	Pass
	500 cycles		Q033747	0/80	1, 2	0/240	
HTSL	JA103		Q034332	0/80	1, 2		
	175°C, 500hr	1 lot, N=>45	Q034327	0/80	1, 2	3 lots	Pass
			Q034326	0/80	1, 2	0/240	
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL	JA108		Q040252	0/100			
	$T_J \geq 125°C$, Dynamic	3 lots, N=>77	Q040423	0/80		3 lots	Pass
	Vcc=5.5V, 1000 hours		Q037715	0/80	3	0/260	
LTOL	JA108						
	-10°C, Dynamic	1 lot, N=>77	Q027145	0/80		1 lots	Pass
	Vcc=5.5V, 1000 hours					0/80	
ELFR	AEC-Q100-008		Q040641	0/807			
	$T_J \geq 125°C$, Dynamic	3 lots, N=>800	Q041004	0/808		3 lots	Pass
	Vcc=5.5V, 48 hours		Q040698	0/808		0/2423	
Test Group C – Package Assembly Integrity Tests							
Wire Bond Shear	AEC-Q100-001		587534.1	0/5	2		
		5 units, N=>30	588405.1	0/5	2	2 lots	Pass
			Q0xxxxx	f/p		0/10	
Wire Bond Pull	M-STD-883		587534.1	0/5	2		
	Performed post-TC	5 units, N=>30	588405.1	0/5	2	2 lots	Pass
			Q0xxxxx	f/p		0/10	
Physical Dimensions	JB100		587534.1	0/30	2		
		3 lots, N=>10	588405.1	0/30	2	2 lots	Pass
			Q0xxxxx	f/p		0/60	
Solderability	JB102		587534.1	0/10	2		
		1 lot, N=>15	588405.1	0/10	2	2 lots	Pass
			Q0xxxxx	f/p		0/20	
Test Group E – Electrical Verification							
ESD-HBM	AEC-Q100-002	1 lot, N=>3	Q040415			5 kV	Class H3A
ESD-CDM	AEC-Q100-011	1 lot, N=>3	Q040416			2500 V	Class C6

Approved by: Noel R. Arguello 1 of 2 Prepared on: 25-Jun-17

Si892x AEC-Q100 Qualification Report

W7101F1 - Product Qualification Report Record Rev. I

Part Rev A, Vanguard Fabrication, UTL Assembly except as noted

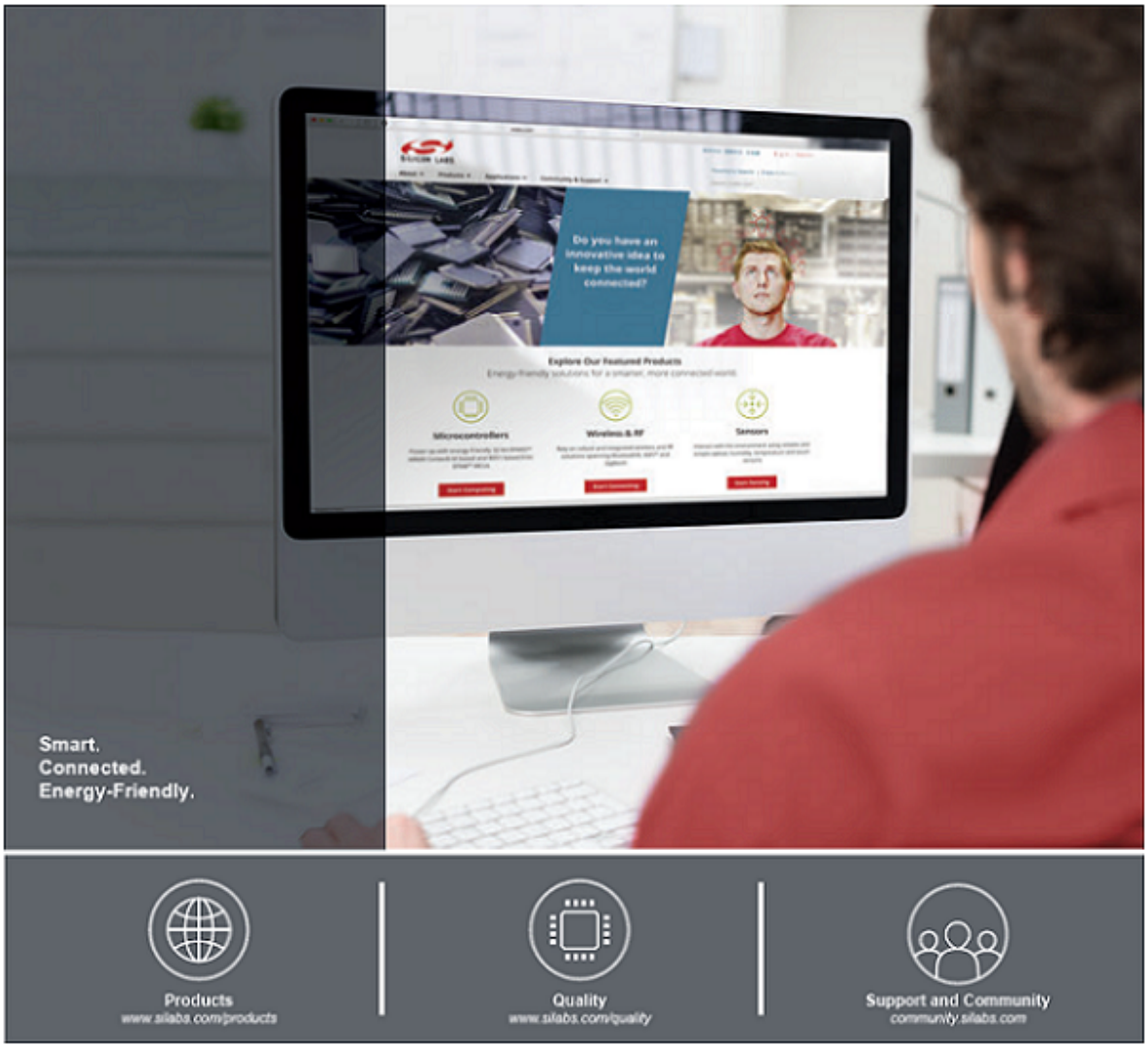
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Latch Up	AEC-Q100-004 ±200mA Overvoltage = 36V	1 lot, N=>6	Q040417	125 °C			Pass

Notes:
1. Parts are Pre-conditioned at MSL3/260°C
2. Leverage package family qualification data
3. Leverage die family qualification data

This report applies to the following part numbers:

Si8920AC-IP	Si8920AC-IPR	Si8920BC-IP	Si8920BC-IPR	Si8920AD-IS
Si8920AD-ISR	Si8920BD-IS	Si8920BD-ISR		

Approved by: Noel R. Arguello 2 of 2 Prepared on: 25-Jun-17



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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

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