TwinDie™ DDR2 SDRAM

MT47H1G4 – 64 Meg x 4 x 8 Banks x 2 Ranks
MT47H512M8 – 32 Meg x 8 x 8 Banks x 2 Ranks

Features

- Uses 2Gb Micron die
- Two ranks (includes dual CS#, ODT, and CKE balls)
- Each rank has 8 internal banks for concurrent operation
- $V_{DD} = V_{DDQ}$ = +1.8V ±0.1V
- JEDEC-standard 63-ball FBGA
- Low-profile package – 1.35mm MAX thickness

Functionality

The 4Gb (TwinDie™) DDR2 SDRAM uses Micron's 2Gb DDR2 monolithic die and has similar functionality. This TwinDie data sheet is intended to provide a general description, package dimensions, and the ballout only. Refer to Micron's 2Gb DDR2 data sheet for complete information or for specifications not included in this document.

Options	Marking
• Configuration	
– 64 Meg x 4 x 8 banks x 2 ranks	1G4
– 32 Meg x 8 x 8 banks x 2 ranks	512M8
• FBGA package (Pb-free)	
– 63-ball FBGA (9mm x 11.5mm) Rev. C	WTR
• Timing – cycle time[1]	
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 2.5ns @ CL = 6 (DDR2-800)	-25
– 3.0ns @ CL = 5 (DDR2-667)	-3
– 3.75ns @ CL = 4 (DDR2-533)	-37E
• Self refresh	
– Standard	None
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 85°C)	None
• Revision	:C

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)				^tRCD (ns)	^tRP (ns)	^tRC (ns)	^tRFC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6				
-25E	400	533	800	800	12.5	12.5	55	197.5
-25	400	533	667	800	15	15	55	197.5
-3	400	533	667	n/a	15	15	55	197.5
-37E	400	533	n/a	n/a	15	15	55	197.5

Table 2: Addressing

Parameter	1 Gig x 4	512 Meg x 8
Configuration	64 Meg x 4 x 8 banks x 2 ranks	32 Meg x 8 x 8 banks x 2 ranks
Refresh count	8K	8K
Row address	A[14:0] (32K)	A[14:0] (32K)
Bank address	BA[2:0] (8)	BA[2:0] (8)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)

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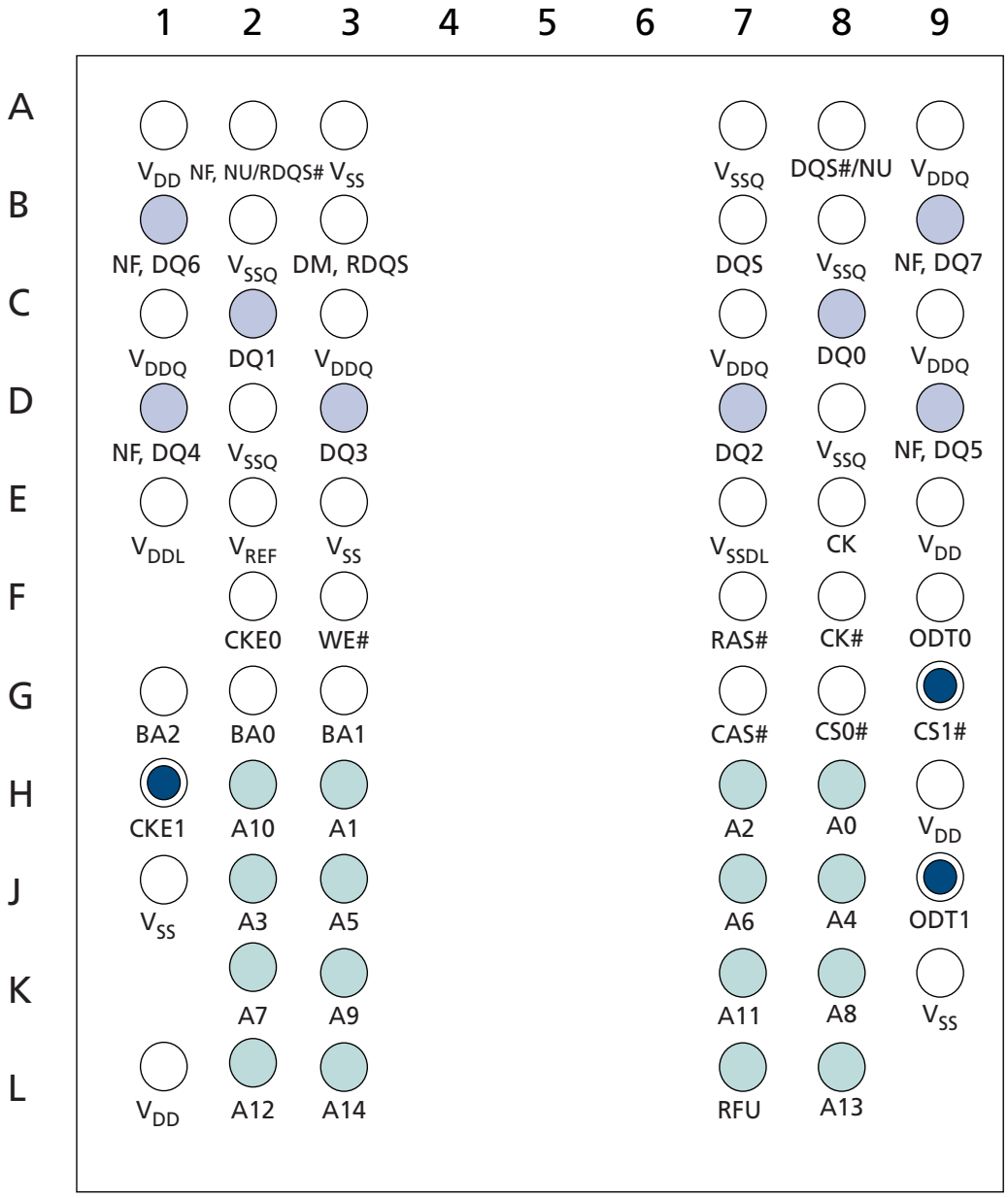
Ball Assignments and Descriptions

Figure 1: 63-Ball FBGA – x4, x8 Ball Assignments (Top View)



Note: 1. Dark balls (with ring) designate balls that differ from the monolithic versions.

Table 3: FBGA 63-Ball Descriptions

Symbol	Type	Description
A[14:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE[1:0]	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, V_{REF} must be maintained.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls.
ODT[1:0]	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for x4 configuration.
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for x8 configuration.
DQS, DQS#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.

Table 3: FBGA 63-Ball Descriptions (Continued)

Symbol	Type	Description
RDQS, RDQS#	I/O	**Redundant data strobe:** For the x8 configuration only. RDQS is enabled/disabled via the load mode command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
V_{DD}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDQ}	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
V_{DDL}	Supply	**DLL power supply:** 1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage (V_{DDQ}/2).
V_{SS}	Supply	Ground.
V_{SSDL}	Supply	**DLL ground:** Isolated on the device from V_{SS} and V_{SSQ}.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NF	–	**No function:** These balls are no function on the x4 configuration.
NU	–	**Not used:** For the x8 configuration only. If EMR(E10) = 0, A2 = RDQS# and A8 = DQS#. If EMR(E10) = 1, A2 and A8 are not used.
RFU	–	Reserved for future use.

Functional Description

The 4Gb (TwinDie) DDR2 SDRAM is a high-speed, CMOS dynamic random access memory device containing 4,294,967,296 bits and internally configured as two 8-bank 2Gb DDR2 SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like-die tested within a monolithic die package.

Each DDR2 SDRAM die uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

Addressing of the TwinDie is identical to the monolithic device. Additionally, multiple chip selects select the desired rank.

This TwinDie data sheet is intended to provide a general description, package dimensions, and the ballout only. Refer to the Micron 2Gb DDR2 data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Functional Block Diagrams

Figure 2: 64 Meg x 4 x 8 Banks x 2 Ranks

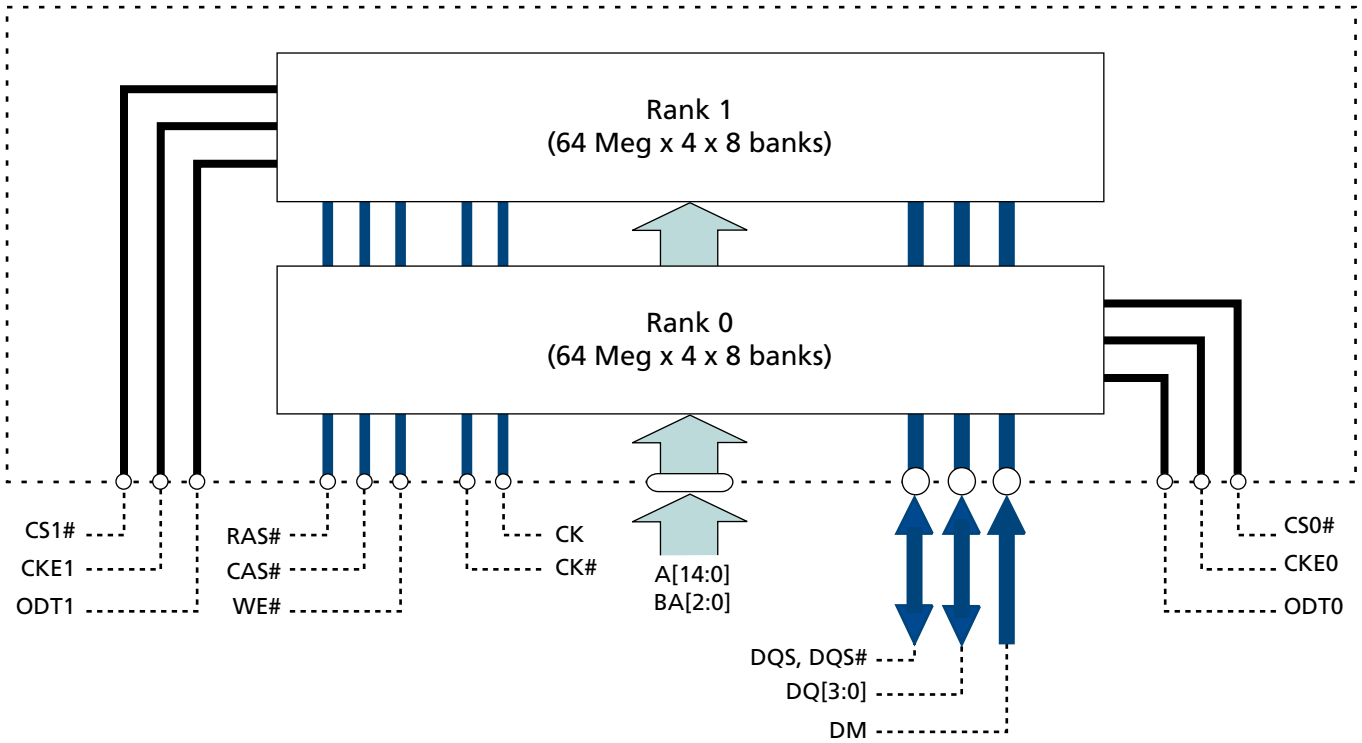
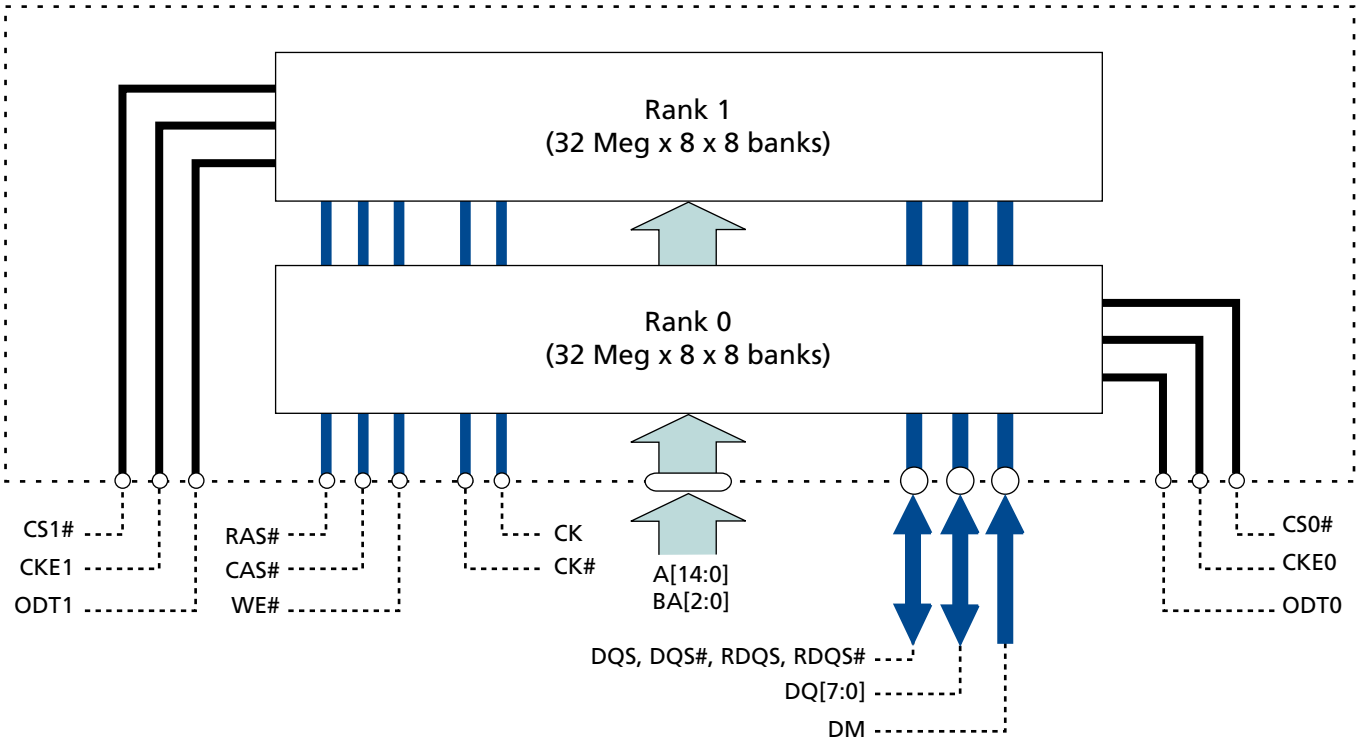


Figure 3: 32 Meg x 8 x 8 Banks x 2 Ranks



Electrical Specifications – Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions oustide those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 4: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	1.0	2.3	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	0.5	2.3	V	1, 2
V_{DDL} supply voltage relative to V_{SSL}	V_{DDL}	0.5	2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	0.5	2.3	V	3
Input leakage current; any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V	I_I	10	10	µA	
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled	I_{OZ}	10	10	µA	
V_{REF} leakage current; V_{REF}= valid V_{REF} level	I_{VREF}	4	4	µA	

Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times; this is not required when power is ramping down.
2. V_{REF} ≤ 0.6 x V_{DDQ}; however, V_{REF} may be ≥ V_{DDQ} provided that V_{REF} ≤ 300mV.
3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 6 (page 10)for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the thermal impedances listed below. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

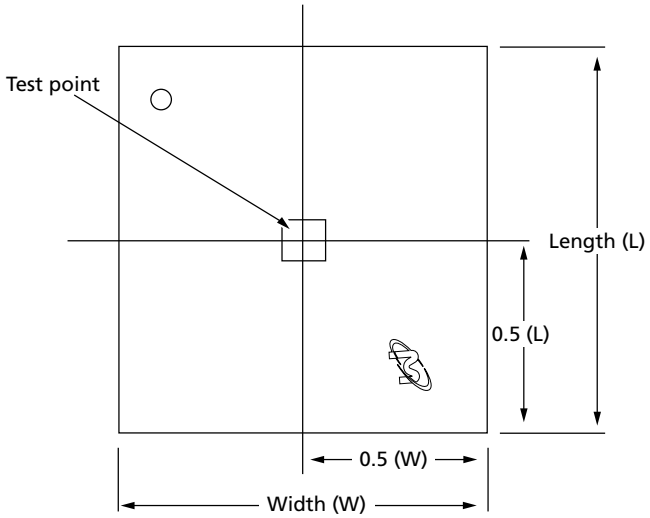
The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Table 5: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	–55	150	°C	1
Operating temperature: commercial	T_C	0	85	°C	2, 3

Notes:
1. MAX storage case temperature T_{STG} is measured in the center of the package, as shown in the figure below. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
2. MAX operating case temperature T_C is measured in the center of the package, as shown below.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.

Figure 4: Example Temperature Test Point Location



Lmm x Wmm FGBA

Table 6: Thermal Impedance

Die Revision	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)	Notes
C	63-ball	2-layer	62.6	45.3	39.2	28.5	3.5	1
		4-layer	45.8	36.5	32.9	28.1		

Note:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Electrical Specifications – I_{CDD} Parameters

Table 7: DDR2 I_{DD} Specifications and Conditions (Die Revision C)

Notes: 1–8 apply to the entire table

Parameter/Condition	Combined Symbol	Individual Die Status	Bus Width	-25E/ -25	-3E/-3	Units
Operating one bank active-precharge current: $^{t}CK = {}^{t}CK$ (I_{DD}), $^{t}RC = {}^{t}RC$ (I_{DD}), $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{CDD2P}$	x4, x8	92	87	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK$ (I_{DD}), $^{t}RC = {}^{t}RC$ (I_{DD}), $^{t}RAS = {}^{t}RAS$ MIN (I_{DD}), $^{t}RCD = {}^{t}RCD$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are switching; Data pattern is same as I_{DD4W} (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{CDD2P}$	x4, x8	107	102	mA
Precharge power-down current: All banks idle; $^{t}CK = {}^{t}CK$ (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{CDD2P}	$I_{CDD2P} = I_{DD2P} + I_{DD2P}$	x4, x8	24	24	mA
Precharge quiet standby current: All banks idle; $^{t}CK = {}^{t}CK$ (I_{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P}$	x4, x8	47	42	mA
Precharge standby current: All banks idle; $^{t}CK = {}^{t}CK$ (I_{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{CDD2P}$	x4, x8	52	47	mA
Active power-down current: All banks open; $^{t}CK = {}^{t}CK$ (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating (individual die status: $I_{CDD3P} = I_{DD3P} + I_{DD2P}$)	I_{CDD3P}	Fast PDN exit MR[12] = 0	x4, x8	42	37	mA
		Slow PDN exit MR[12] = 1	x4, x8	26	26	
Active power-down current: All banks open; $^{t}CK = {}^{t}CK$ (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating (individual die status: $I_{CDD3P} = I_{DD3P} + I_{DD2P}$)	I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{CDD2P}$	x4, x8	62	57	mA
Active standby current: All banks open; $^{t}CK = {}^{t}CK$ (I_{DD}), $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{CDD2P}$	x4, x8	162	142	mA
Operating burst read current: All banks open, continuous burst reads, Iout = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^{t}CK = {}^{t}CK$ (I_{DD}), $^{t}RAS = {}^{t}RAS$ MAX (I_{DD}), $^{t}RP = {}^{t}RP$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{CDD2P}$	x4, x8	162	142	mA

Table 7: DDR2 I_{DD} Specifications and Conditions (Die Revision C) (Continued)

Notes: 1–8 apply to the entire table

Parameter/Condition	Combined Symbol	Individual Die Status	Bus Width	-25E/ -25	-3E/-3	Units
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; refresh command at every $^{t}RFC(I_{DD})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD5}	$I_{CDD5} = I_{DD5} + I_{CDD2P}$	x4, x8	197	177	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{CDD6}	$I_{CDD6} = I_{DD6} + I_{DD6}$	x4, x8	24	24	mA
Operating bank interleave read current: All bank interleaving reads, Iout = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^{t}RCD (I_{DD})$ - 1 x $^{t}CK (I_{DD})$; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RRD = {}^{t}RRD (I_{DD})$, $^{t}RCD = {}^{t}RCD$ (Idd); CKE is HIGH, CS# is HIGH between valid commands; address bus inputs are stable during deselects; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD7}	$I_{CDD7} = I_{DD7} + I_{CDD2P}$	x4, x8	262	237	mA

Notes:

1. I_{CDD}/I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C. $V_{DD} = V_{DDQ}$ = +1.8V ±0.1V; V_{DDL} = +1.8V ±0.1V; $V_{REF} = V_{DDQ}/2$.
2. I_{CDD}/I_{DD} parameters are specified with ODT disabled.
3. Data bus consists of DQ, DM, DQS, DQS#, RDQS, and RDQS#. Idd values must be met with all combinations of EMR bits 10 and 11.
4. I_{CDD}/I_{DD}values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for I_{CDD}/I_{DD} conditions:

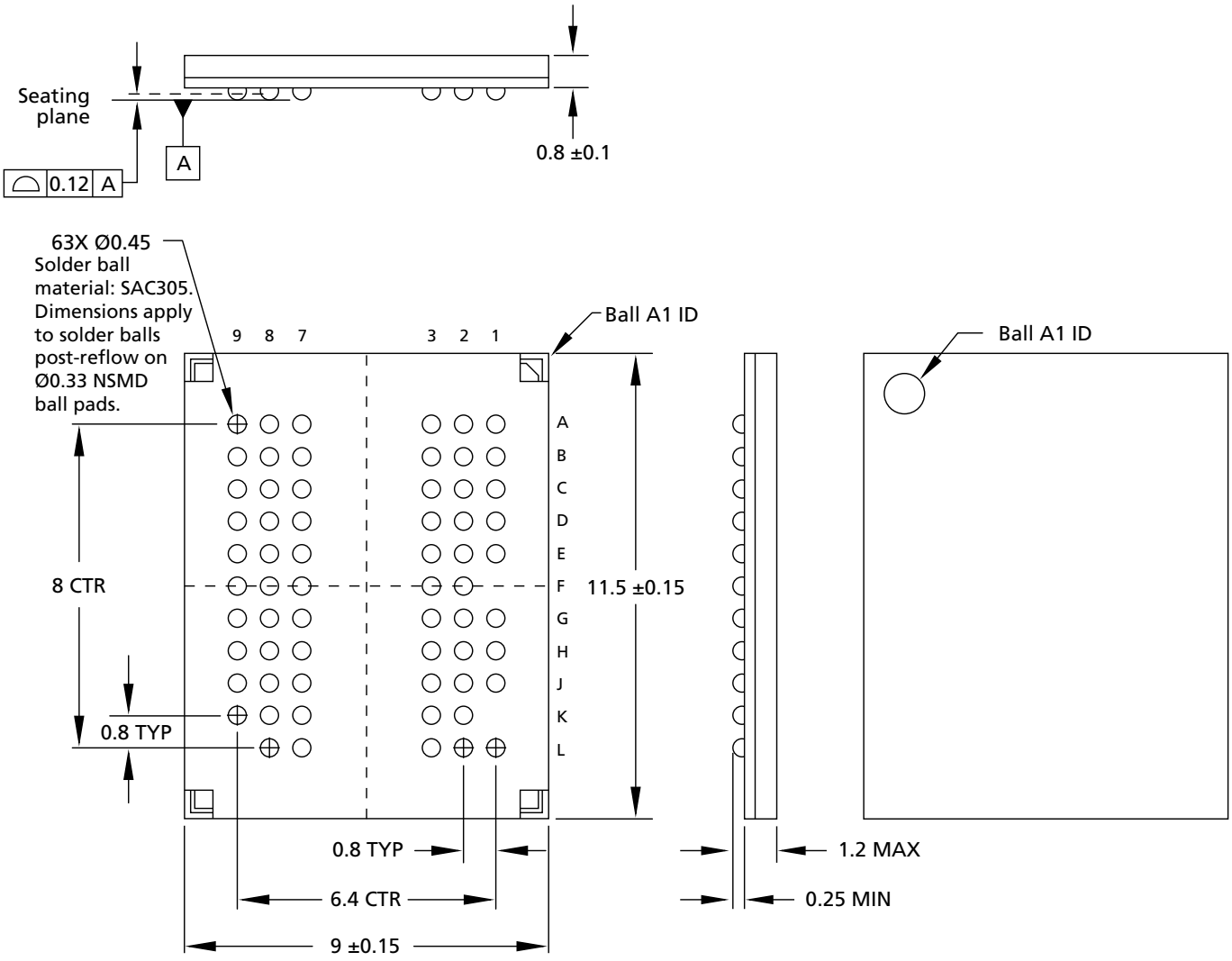
LOW	$V_{IN(AC)} \le V_{IL(AC)max}$
HIGH	$V_{IN} \ge V_{IH(AC)min}$
Stable	Inputs stable at a HIGH or LOW level
Floating	Inputs at $V_{REF} = V_{DDQ}/2$
Switching	Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
Switching	Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes

6. I_{DD1}, I_{DD4R}, and I_{DD7} require A12 in EMR1 to be enabled during testing.
7. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.
8. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option or on AT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:

When T_C ≤ 0°C	I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD5W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%
When T_C ≥ 85°C	I_{DD0} , I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5W} must be derated by 2%; I_{DD2P} must be derated by 20%; I_{DD3P} slow must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2X refresh option is still enabled)

Package Dimensions

Figure 5: 63-Ball FBGA (9mm x 11.5mm) (WTR)



Note: 1. All dimensions are in millimeters.