Complete DDR Memory Power Supply Controller

General Description

The RT8248A provides a complete power supply for DDR2/DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 memory systems. It integrates a synchronous PWM Buck controller with a 1.5A sink/source tracking linear regulator and buffered low noise reference.

The PWM controller provides the low quiescent current, high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage chipset RAM supplies in notebook computers. The constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8248A achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The Buck conversion allows this device to directly step down high-voltage batteries for the highest possible efficiency.

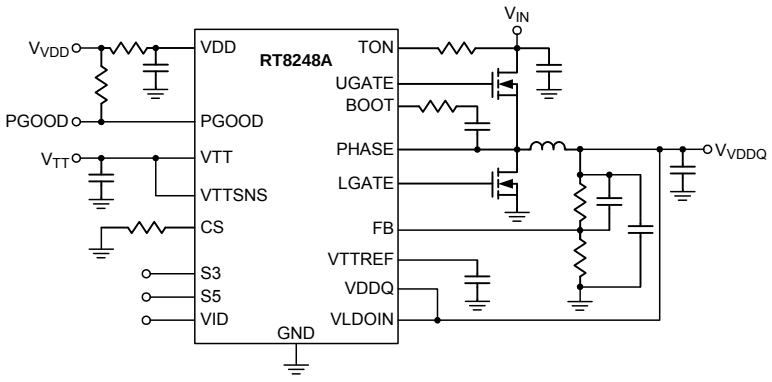
The 1.5A sink/source LDO maintains fast transient response only requiring a 10µF ceramic output capacitor. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The IC supports all of the sleep state controls placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

The RT8248A provides protections including OVP, UVP, and thermal shutdown and available in the WQFN-20L 3x3 package.

Features

- **PWM Controller**
  - **Adjustable Current Limit with Low-Side $R_{DS(ON)}$ Sensing**
  - **Low Quiescent Supply Current**
  - **Quick Load-Step Response within 100ns**
  - **1% V_{VDDQ} Accuracy Over Line and Load**
  - **Adjustable 0.675V to 3.3V Output Range for 1.8V (DDR2), 1.5V (DDR3), 1.35V (DDR3L), 1.2V (LPDDR3), 1.2V (DDR4) and 1.1V (LPDDR4)**
  - **4.5V to 26V Battery Input Range**
  - **Resistor Adjustable Frequency**
  - **Over-/Under-Voltage Protection**
  - **Internal Voltage Ramp Soft-Start**
  - **Drives Large Synchronous Rectifier MOSFETs**
  - **Power Good Indicator**
- **1.5A LDO (VTT), Buffered Reference (VTTREF)**
  - **Capable to Sink and Source Up to 1.5A**
  - **LDO Input Available to Optimize Power Losses**
  - **Requires Only 10µF Ceramic Output Capacitor**
  - **Integrated Divider Tracks 1/2 VDDQ for both VTT and VTTREF**
  - **Accuracy ±20mV for both VTTREF and VTT**
  - **Supports High-Z in S3 and Soft-Off in S4/S5**

Simplified Application Circuit

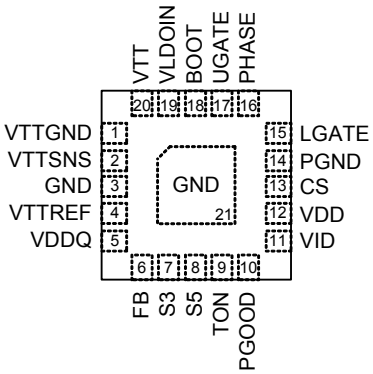


Applications

- DDR2/DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 Memory Power Supplies
- Notebook computers
- SSTL18, SSTL15 and HSTL bus termination

Pin Configuration

(TOP VIEW)



WQFN-20L 3x3

Ordering Information

RT8248A□□

- Package Type
  QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

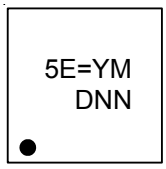
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8248AGQW



5E= : Product Code

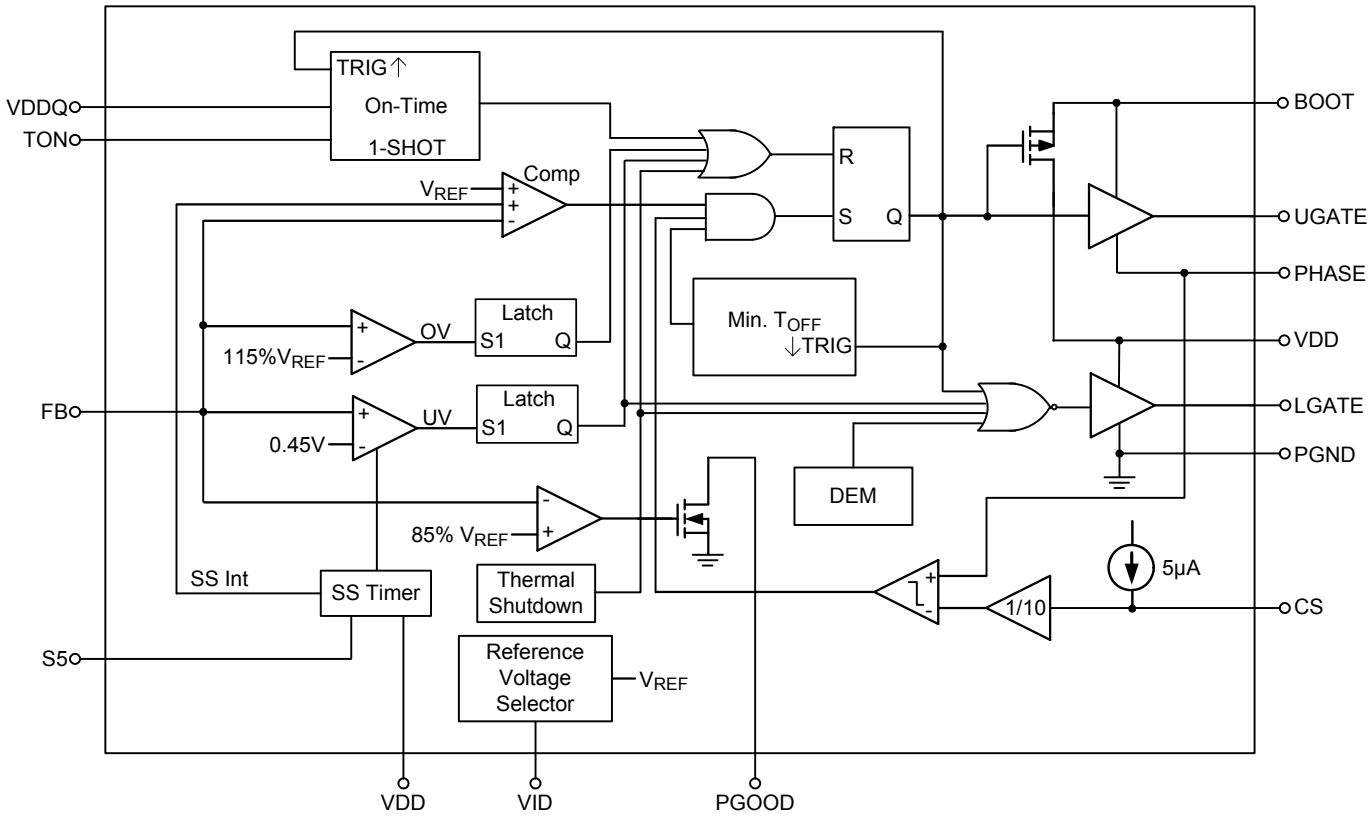
YMDNN : Date Code

Functional Pin Description

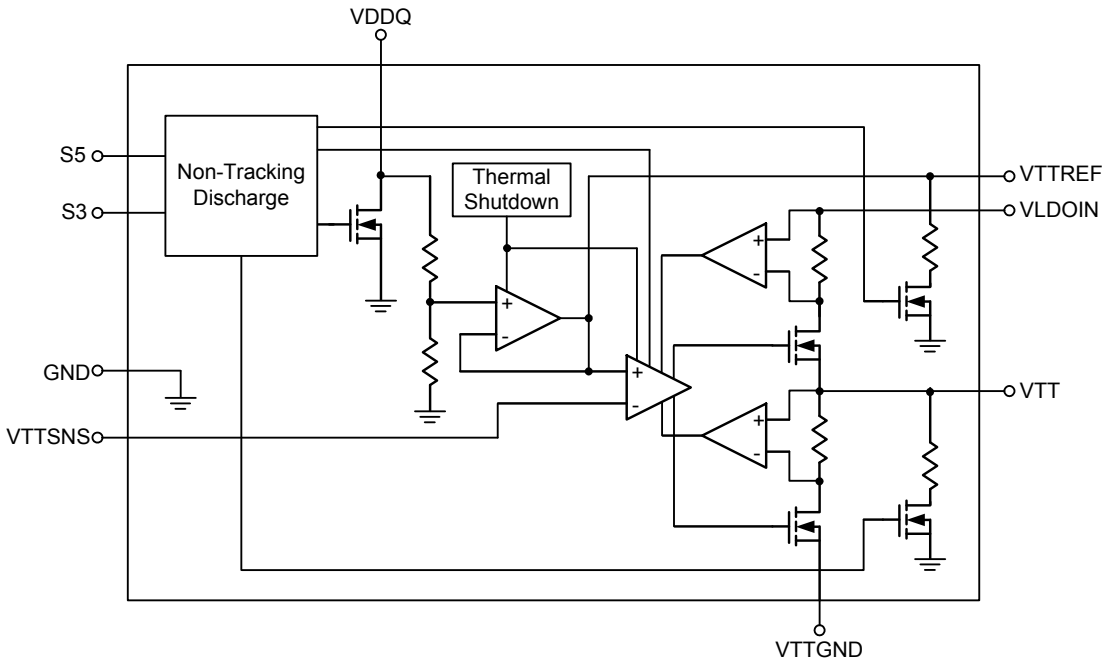
Pin No.	Pin Name	Pin Function
1	VTTGND	Power ground for the VTT LDO.
2	VTTSNS	Voltage sense input for the VTT LDO. Connect to the terminal of the VTT_LDO output capacitor.
3, 21 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	VTTREF	VTTREF buffered reference output.
5	VDDQ	Reference input for VTT and VTTREF.
6	FB	Feedback voltage input. Connect to a resistive voltage divider from VDDQ to GND to adjust the output voltage.
7	S3	VTT LDO enable control input. Do not leave this pin floating.
8	S5	PWM enable control input. Do not leave this pin floating.
9	TON	Set the UGATE on-time through a pull-up resistor connecting to VIN.
10	PGOOD	Power good open-drain output. In high state when VDDQ output voltage is within the target range.
11	VID	Internal reference voltage setting.
12	VDD	Supply voltage input for the analog supply and LGATE gate driver.
13	CS	Current limit threshold setting input. Connect to GND through the voltage setting resistor.
14	PGND	Power ground for low-side MOSFET.
15	LGATE	Low-side gate driver output for VDDQ.
16	PHASE	Switch node. External inductor connection for VDDQ and behave as the current sense comparator input for Low-Side MOSFET $R_{DS(ON)}$ sensing.
17	UGATE	High-side gate driver output for VDDQ.
18	BOOT	Bootstrap supply for high-side gate driver.
19	VLDOIN	Power supply for VTT LDO.
20	VTT	Power output for the VTT LDO.

Functional Block Diagram

Buck Controller



VTT LDO



Operation

The RT8248A is a constant on-time synchronous step-down controller. In normal operation, the high-side N-MOSFET is turned on when the output voltage is lower than VREF, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Soft-Start (SS)

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture. When the soft-start is finished, the PGOOD open-drain output will be high impedance.

Current Limit

The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The current limit threshold can be set with an external voltage setting resistor on the CS pin.

Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

The output voltage is continuously monitored for over-voltage and under-voltage protection. When the output voltage exceeds its set voltage threshold(115% of V_{OUT}), UGATE goes low and LGATE is forced high. When the feedback voltage is less than 0.45V, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until VDD is re-supplied and exceeds the POR rising threshold voltage or S5 is reset.

VTT Linear Regulator and VTTREF

This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough for keeping track of VTTREF within 40mV at all conditions, including fast load transient. The VTTREF block consists of on-chip 1/2 divider, LPF and buffer. This regulator also has sink and source capability up to 10mA. Bypass VTTREF to GND with a 33nF ceramic capacitor for stable operation.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, TON to GND ---------- –0.3V to 32V
- BOOT to GND
  - DC ---------- –0.3V to 38V
  - < 100ns ---------- –5V to 42V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 20ns ---------- –8V to 38V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –2.5V to 7.5V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- VDD, CS, S3, S5, VTTSNS, VDDQ, VID, VTTREF, VTT, VLDOIN, FB, PGOOD to GND ---------- –0.3V to 6V
- PGND, VTTGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 4.5V to 26V
- Control Voltage, VDD ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 5V, V_{IN} = 12V, R_{TON} = 620kΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current		FB forced above the regulation point, V_{S5} = 5V, V_{S3} = 0V, not switching	--	135	--	μA
TON Operating Current		R_{TON} = 620kΩ, V_{IN} = 12V	--	19	--	μA
I_{VLDOIN} BIAS Current		V_{S5} = V_{S3} = 5V, VTT = no load	--	1	--	μA
I_{VLDOIN} Standby Current		V_{S5} = 5V, V_{S3} = 0, VTT = no load	--	0.1	10	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current (V_{S5} = V_{S3} = 0V)	I_{SHDN}	VDD	--	0.1	10	μA
		TON	--	0.1	5	μA
		S5/S3	–1	0.1	1	μA
		VLDOIN	--	0.1	1	μA
		VID	--	0.5	1	μA
FB Error Comparator Threshold	V_{REF}	V_{REF} = 0.675V/0.75V	–1	0	1	%
VDDQ Voltage Range			0.675	--	3.3	V
Switch Frequency	f_{SW}	R_{TON} = 620k, V_{IN} = 12V, V_{DDQ} = 1.5V, I_{OUT} = 20A (Note 5)	320	400	480	kHz
Minimum Off-Time			250	400	550	ns
VDDQ Shutdown Discharge Resistance		V_{S5} = 0V, V_{S3} = 0V	--	15	--	Ω
Current Sensing						
CS Pin Source Current			4.5	5	5.5	μA
Zero Crossing Threshold		GND – PHASE	–2	--	10	mV
Fault Protection						
Current Limit (Positive)		GND – PHASE, R_{CS} = 160kΩ	70	80	90	mV
Output UV Threshold	V_{UVP}	V_{FB} falling. For both VID is high or low.	0.4	0.45	0.5	V
UVP Latch Delay		FB forced below UV threshold	--	30	--	μs
OVP Threshold	V_{OVP}	With Respect to Error Comparator Threshold	110	115	120	%
OVP Latch Delay		FB forced above OV threshold	--	5	--	μs
VDD POR Threshold		Rising edge, hysteresis = 120mV, PWM disabled below this level	3.9	4.2	4.5	V
Voltage Ramp Soft-Start Time		From S5 going high to V_{FB} = 0.675V	--	1	--	mS
UV Blank Time		From S5 signal going high	--	5	--	mS
Thermal Shutdown	T_{SD}		--	165	--	°C
Driver On-Resistance						
UGATE Gate Driver Source	$R_{UGATEsr}$	BOOT – PHASE forced to 5V	--	2.5	5	Ω
UGATE Gate Driver Sink	$R_{UGATEsk}$	BOOT – PHASE forced to 5V	--	1.5	3	Ω
LGATE Gate Driver Source	$R_{LGATEsr}$	DL, high state	--	2.5	5	Ω
LGATE Gate Driver Sink	$R_{LGATEsk}$	DL, low state	--	0.8	1.6	Ω
Dead Time		LGATE rising (Phase = 1.5V)	--	40	--	ns
		UGATE rising	--	40	--	
Internal Boost Charging Switch On-Resistance		VDD to BOOT, 10mA	--	--	80	Ω

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Logic I/O							
S3, S5 Input Voltage	Logic-High			2	--	--	V
	Logic-Low			--	--	0.8	
Logic Input Current			S3, S5 = VDD / GND	–1	0	1	μA
VID Input Threshold Voltage	Logic-High			750	--	--	mV
	Logic-Low			--	--	300	
PGOOD (Upper Side Threshold Decide by OV Threshold)							
Trip Threshold (Falling)			Measured at FB, with respect to reference, no load. hysteresis = 2%	–20	–15	–10	%
Fault Propagation Delay			Falling edge, FB forced below PGOOD trip threshold	--	5	--	μs
Output Low Voltage			I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		I_{LEAK}	High state, forced to 5V	--	--	1	μA
VTT LDO							
VTT Output Tolerance		V_{VTTTOL}	V_{DDQ} = V_{LDOIN} = 1.2V/1.35V/1.5V/1.8V, $\|I_{VTT}\|$ = 0A	–20	--	20	mV
			V_{DDQ} = V_{LDOIN} = 1.2V/1.35V/1.5V/1.8V, $\|I_{VTT}\|$ < 1A	–30	--	30	
			V_{DDQ} = V_{LDOIN} = 1.2V/1.35V, $\|I_{VTT}\|$ < 1.2A	–40	--	40	
			V_{DDQ} = V_{LDOIN} = 1.5V/1.8V, $\|I_{VTT}\|$ < 1.5A	–40	--	40	
VTT Source Current Limit		$I_{VTTOCLSRC}$	V_{TT} = 0V	1.6	2.6	3.6	A
VTT Sink Current Limit		$I_{VTTOCLSNK}$	V_{TT} = V_{DDQ}	1.6	2.6	3.6	A
VTT Leakage Current		I_{VTTLK}	S5 = 5V, S3 = 0V, VTT = $\left(\frac{V_{VDDQ}}{2}\right)$	–10	--	10	μA
VTTSNS Leakage Current		$I_{VTTSNSLK}$	I_{SINK} = 1mA	–1	--	1	μA
VTT Discharge Current		I_{DSCHRG}	V_{DDQ} = 0V, V_{TT} = 0.5V, S5 = S3 = 0V	10	30	--	mA
VTTREF Output Voltage		V_{VTTREF}	V_{VTT} = V_{VTTREF} = $\left(\frac{V_{VDDQ}}{2}\right)$, V_{VDDQ} = 1.5V	--	0.75	--	V
VDDQ/2, VTTREF Output Voltage Tolerance		$V_{VTTREFTOL}$	V_{LDOIN} = V_{VDDQ} = 1.5V, $\|I_{VTTREF}\|$ < 10mA	–15	--	15	mV
			V_{LDOIN} = V_{VDDQ} = 1.8V, $\|I_{VTTREF}\|$ < 10mA	–18	--	18	
VTTREF Source Current Limit		$I_{VTTREFOCL}$	V_{VTTREF} = 0V	10	40	80	mA

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Not production tested. Test condition refer to electrical characteristics using application circuit.

Typical Application Circuit

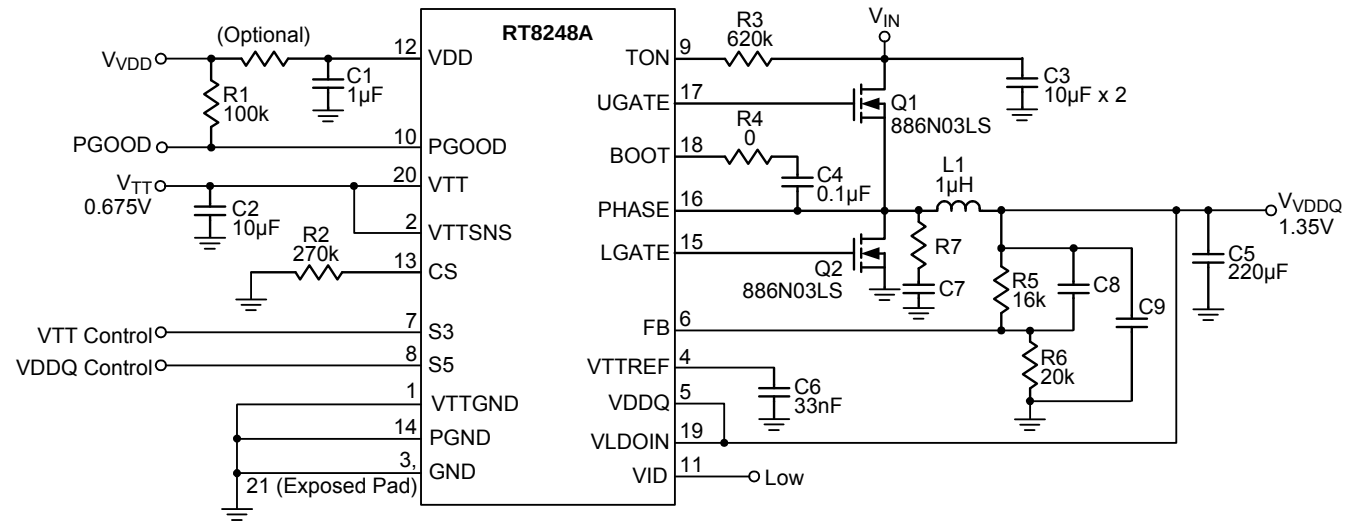


Figure 1. Typical Application Circuit with POSCAP Solution

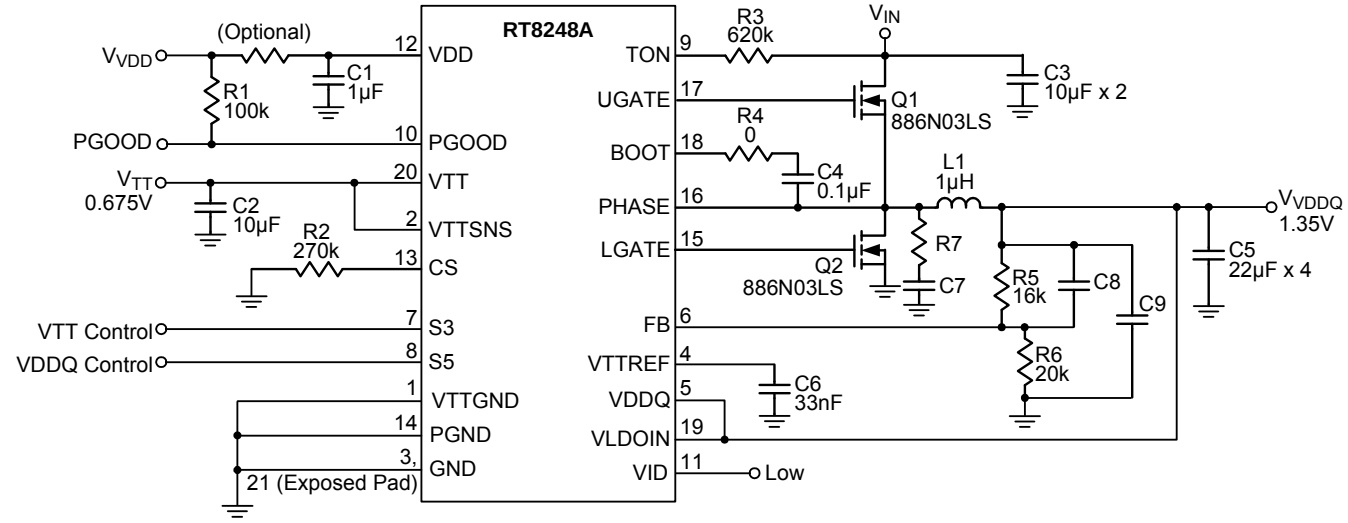
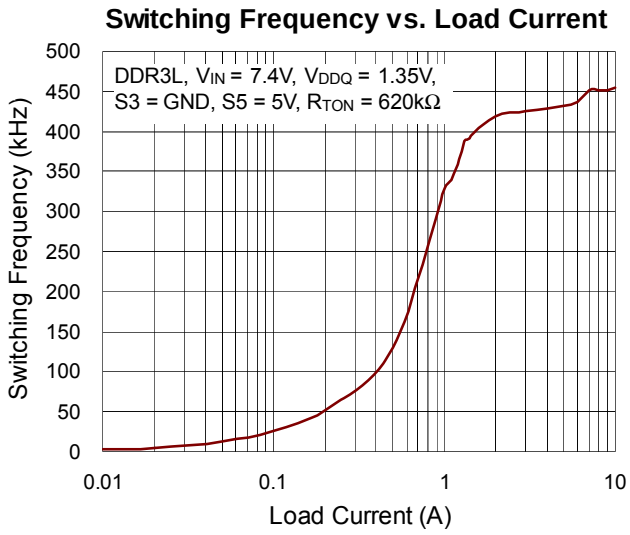
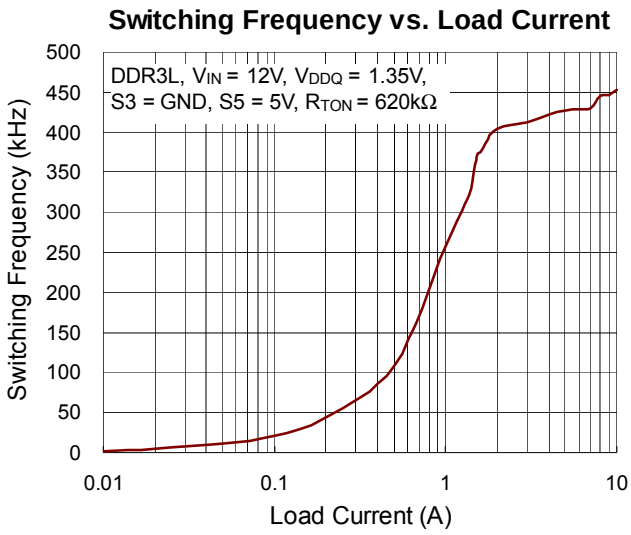
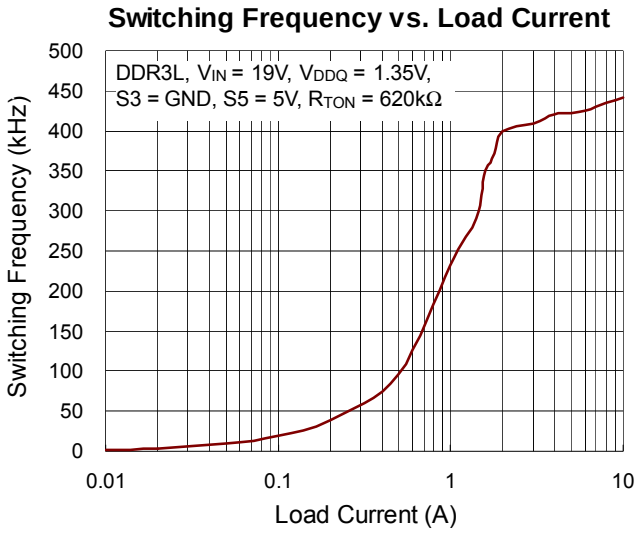


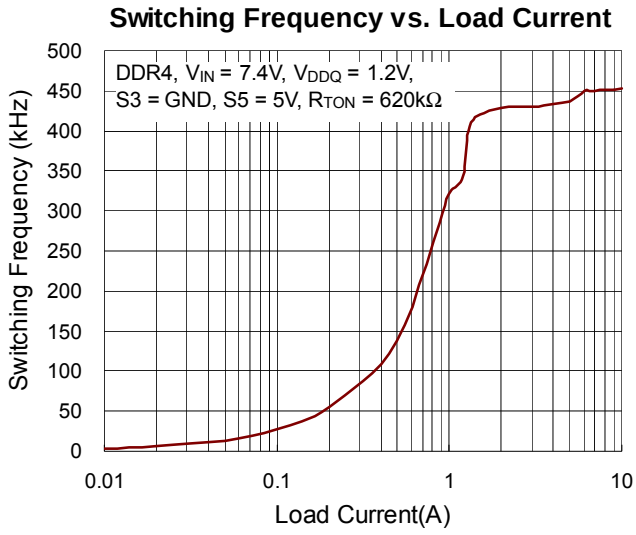
Figure 2. Typical Application Circuit with Pure MLCC Solution

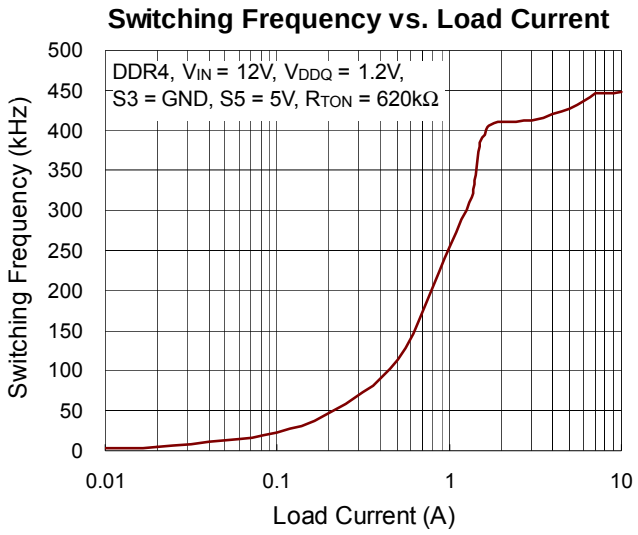
Typical Operating Characteristics

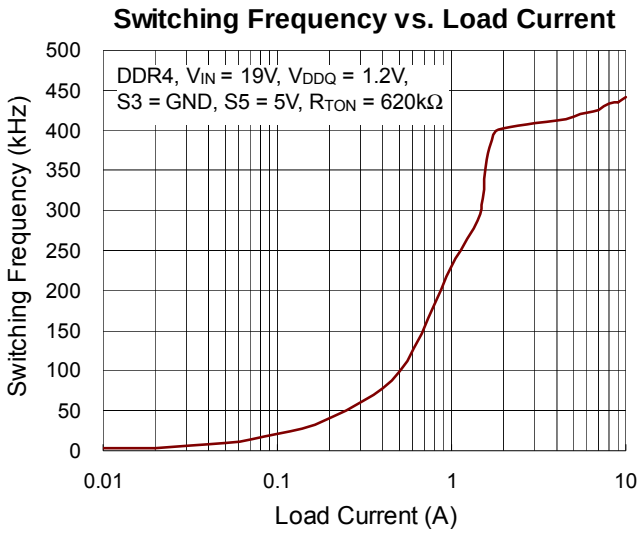




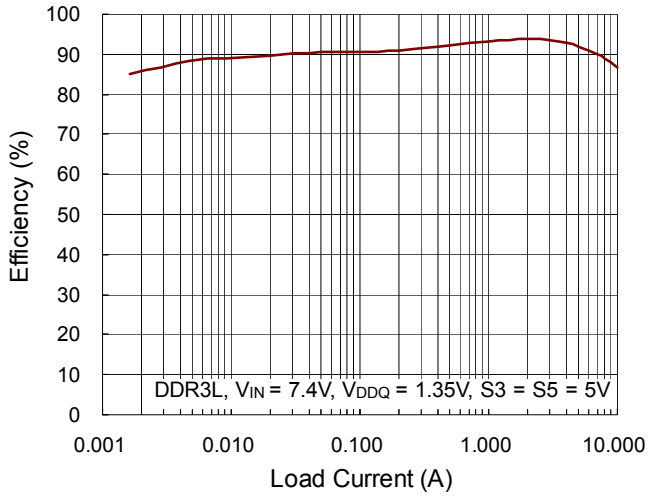








Efficiency vs. Load Current



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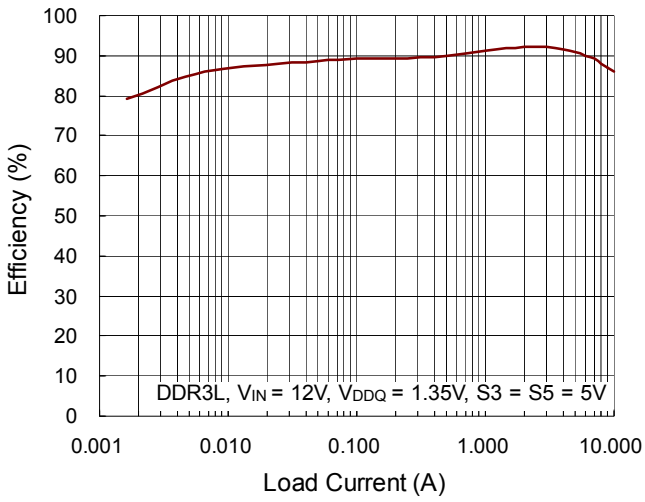

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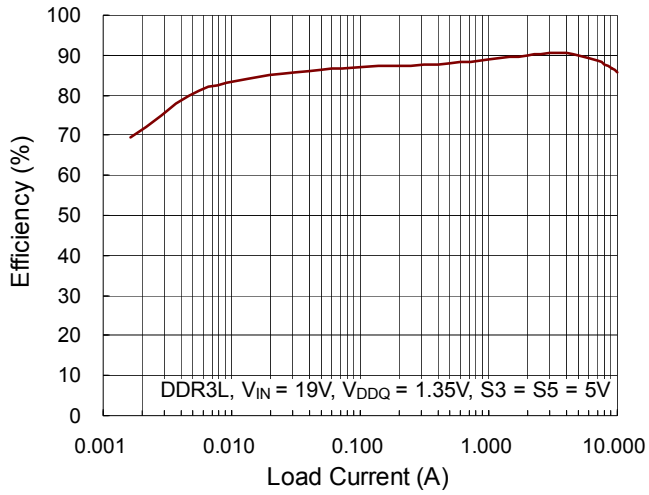

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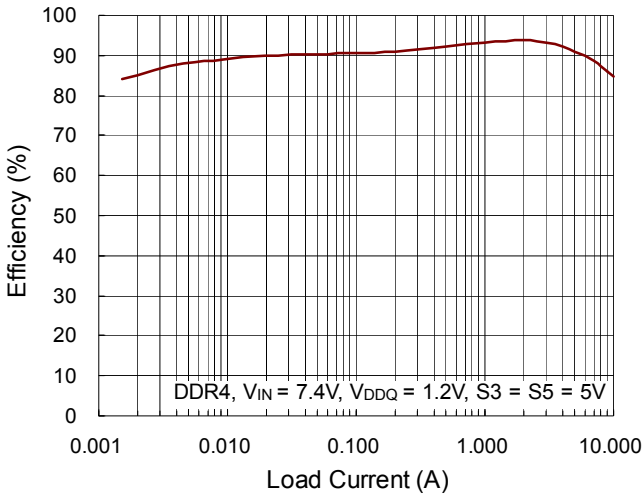

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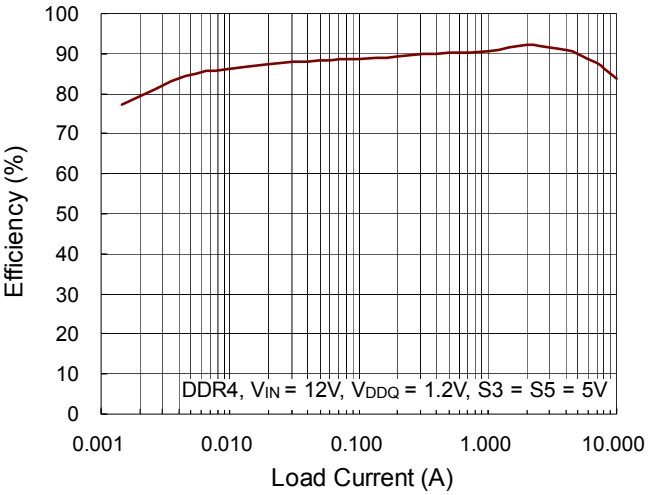

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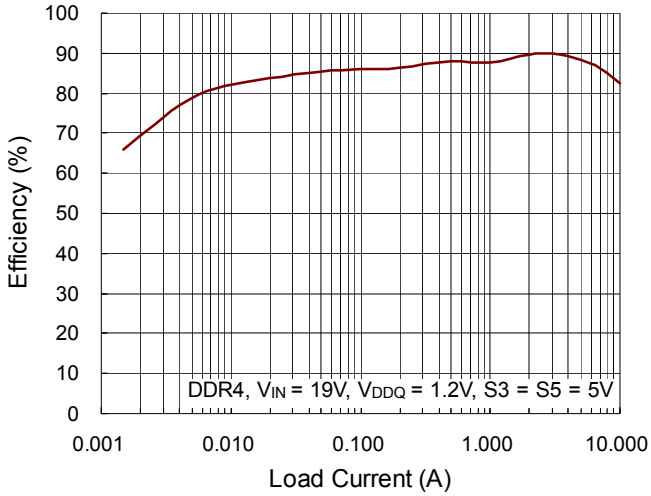
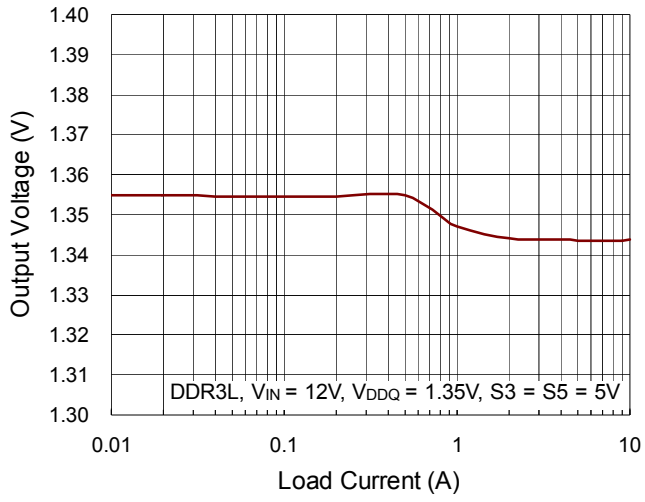
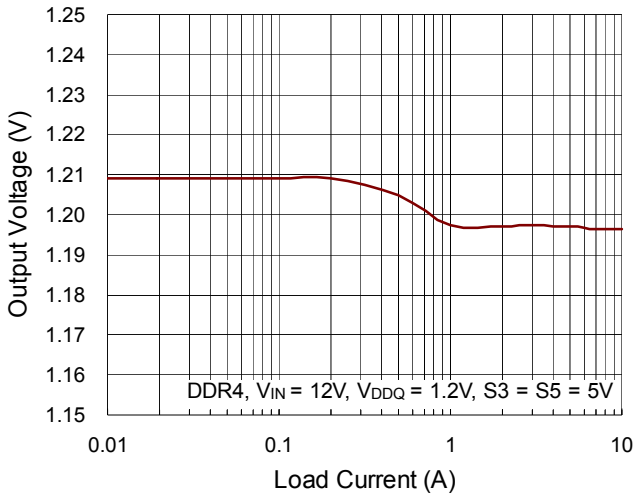


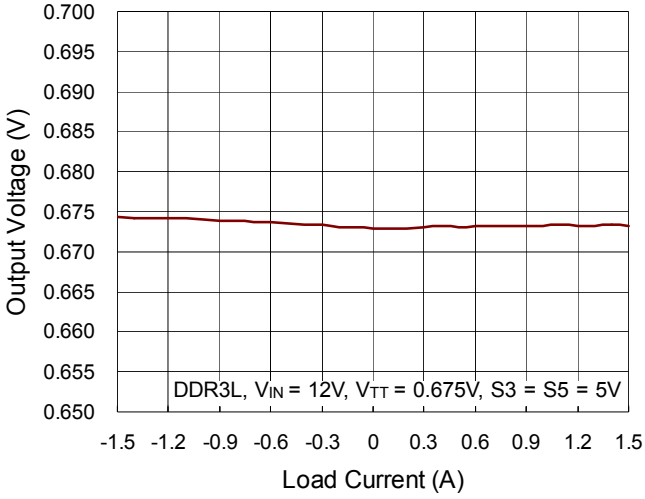
VDDQ Output Voltage vs. Load Current



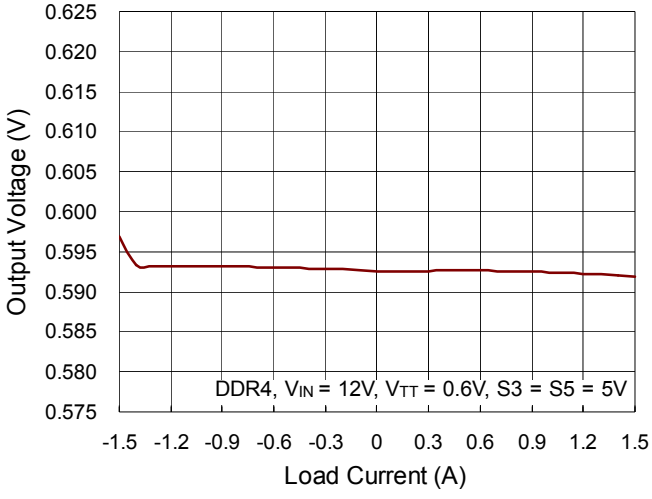
VDDQ Output Voltage vs. Load Current



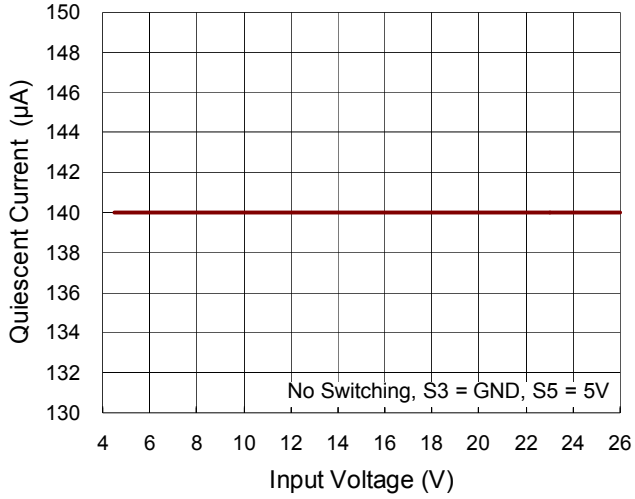
VTT Output Voltage vs. Load Current



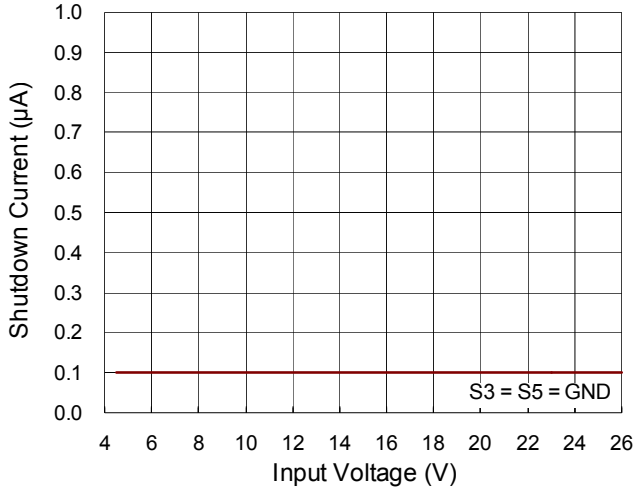
VTT Output Voltage vs. Load Current



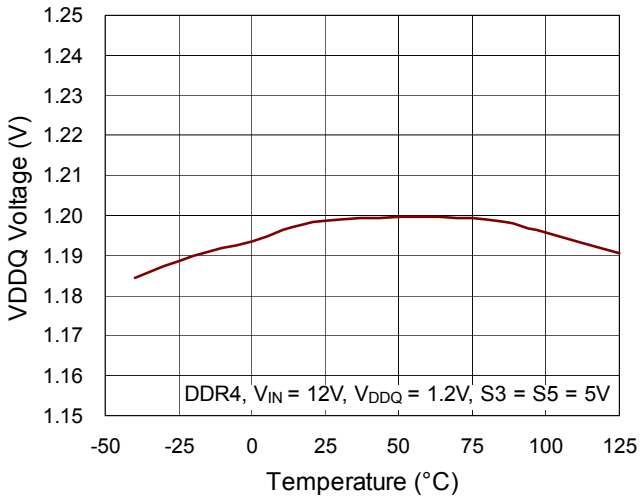
Quiescent Current vs. Input Voltage



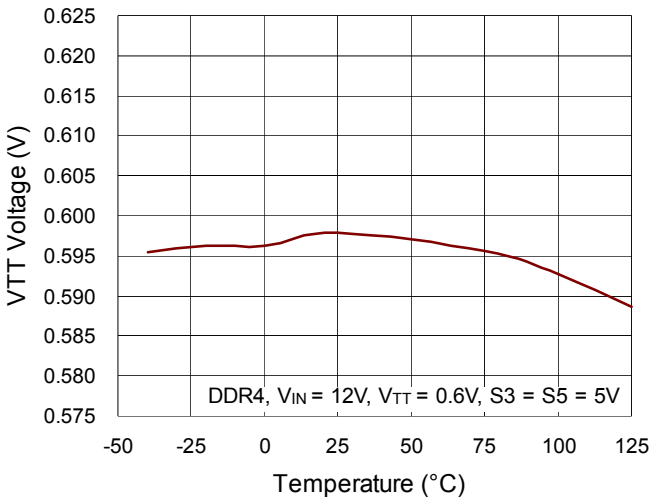
Shutdown Current vs. Input Voltage



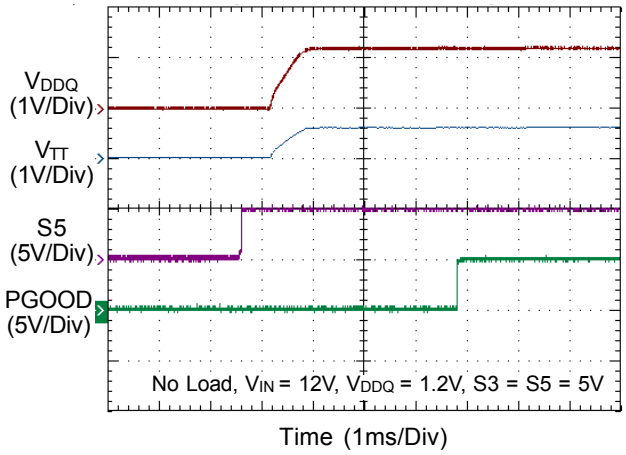
VDDQ Voltage vs. Temperature



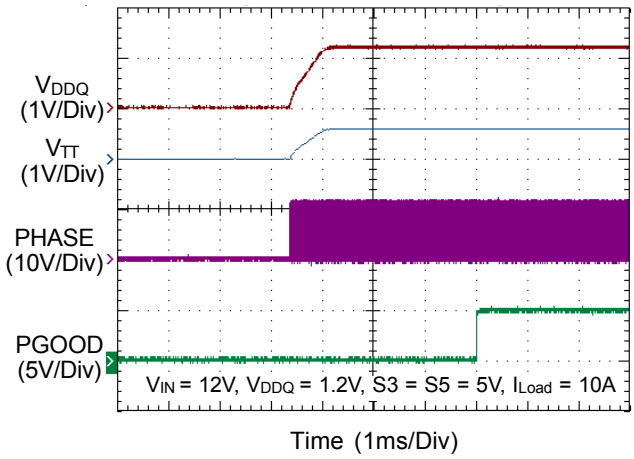
VTT Voltage vs. Temperature



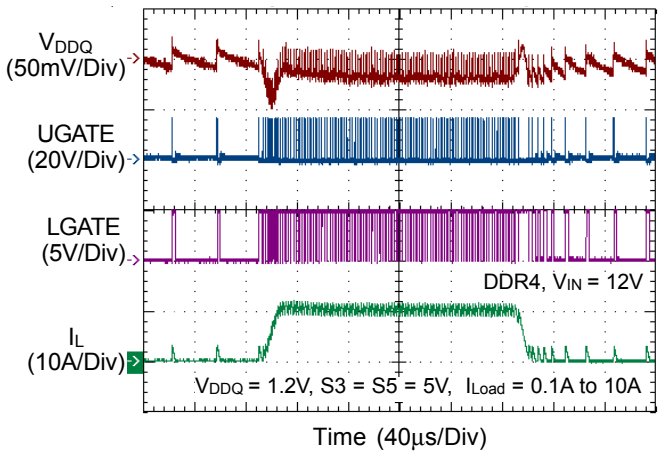
VDDQ and VTT Start Up



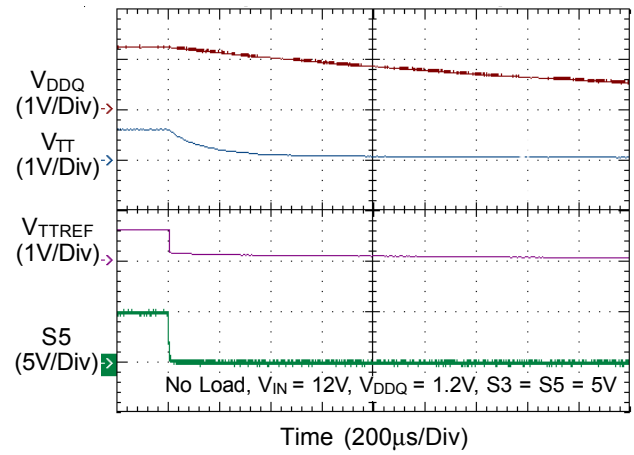
VDDQ Start Up



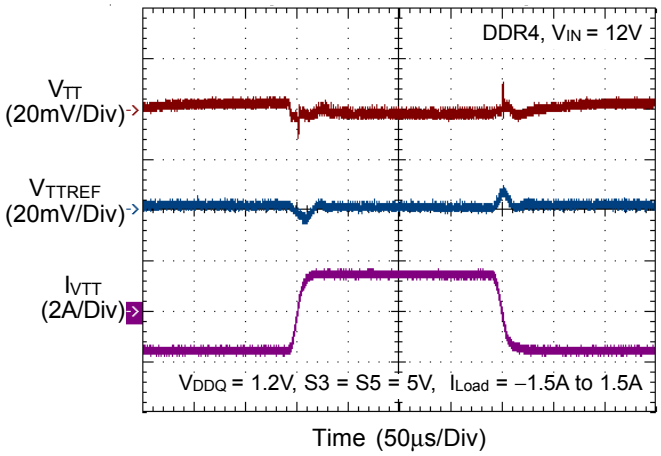
VDDQ Load Transient Response



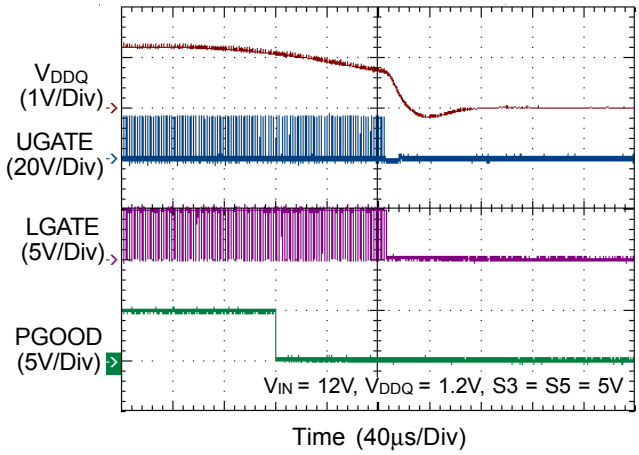
Non-Tracking Discharge Shutdown



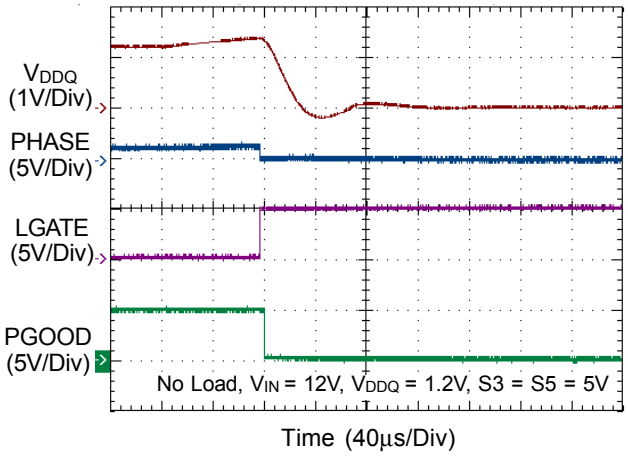
VTT Load Transient Response



Under Voltage Protection



Over Voltage Protection



Application Information

The RT8248A PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage chipset RAM supplies in notebook computers. Richtek's Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology solves the poor load transient response timing problems of fixed-frequency current mode PWMs, and avoids problems caused by widely varying switching frequencies in conventional constant-on-time and constant- off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

The 1.5A sink/source LDO maintains fast transient response, only requiring 10μF of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The RT8248A supports all of the sleep state controls, placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Referring to the function block diagrams of the RT8248A, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one-shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{VDDQ}, thereby making the on-time of the high-side switch directly proportional to the output voltage and inversely proportional to the input voltage. This implementation results in a nearly constant switching frequency without the need of a clock generator, as shown below :

$$t_{ON} = 3.85p \times R_{TON} \times V_{VDDQ} / [(V_{IN} - 0.5) + R_{TON} \times 1\mu]$$

And then the switching frequency is :

$$f = V_{VDDQ} / (V_{IN} \times t_{ON})$$

where R_{TON} is the resistor connected from V_{IN} to the TON pin. Note that the setting on-time must be longer than 100ns (typ.) of the minimum on-time and shorter than 3μs (typ.) of the maximum on-time.

Diode Emulation Mode

In diode emulation mode, the RT8248A automatically reduces switching frequency at light load conditions to maintain high efficiency. As the output current decreases from heavy load condition, the inductor current will also be reduced and eventually come to the point where its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In contrast, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light load operation is shown in Figure 3 and can be calculated as follows :

$$I_{LOAD(SKIP)} \approx \frac{V_{IN} - V_{VDDQ}}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

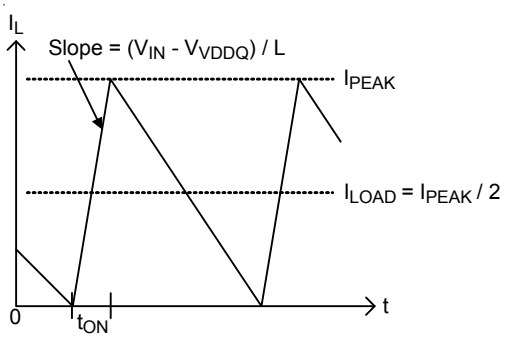


Figure 3. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light load causes diode-emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade offs in DEM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

Selection of $R_{DS(ON)}$ and Inductance

The current signal is sensed by low side MOSFET. Both ZCD and OCP require accurate current signal for correct function. Since the current sensing tolerance for zero current detection is from –2mV to 10mV as defined in the EC table, which means the error of ZCD is unavoidable. However, the error rate can be controlled with proper selection of $R_{DS(ON)}$ and inductance. The error rate of ZCD can be calculated by following equation :

$$ZCD\_error = \frac{ZCD\_tolerance}{R_{DS(ON)}} \times \frac{1}{\Delta I_L} \times 100\%$$

, where ZCD_telerance = –2mV to10mV.

In order to confirm the ZCD function is available, the minimum value of $R_{DS(ON)}$ should be larger than 2mV/(ΔL/2). It should be known that both $R_{DS(ON)}$ and inductance are important in the equation.

On the other hand, OCP level is adjusted by external resistor, R_{LIMIT}. The OCP level should always be larger than upper ZCD_tolerance value. That is, V_{CS} / 10 > 10mV is necessary to confirm the correct OCP function. V_{CS} is the current limit threshold decided by R_{LMIT}, the equation can be found in following section.

Current Limit Setting for VDDQ (CS)

The RT8248A provides cycle-by-cycle current limit control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery and output voltage.

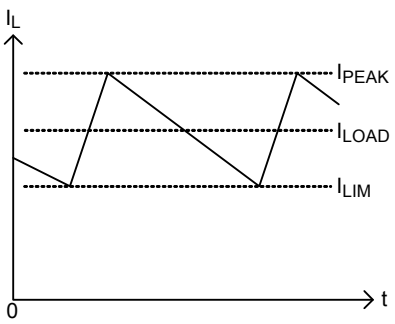


Figure 4. "Valley" Current Limit

The RT8248A uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The setting resistor, R_{ILIM}, between the CS pin and VDD sets the current limit threshold. The CS pin sources an internal 5μA (typ.) current source at room temperature. This current has a 4700ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(ON)}$. When the voltage drop across the low-side MOSFET equals the voltage across the R_{ILIM} setting resistor, the positive current limit will activate. The high-side MOSFET will not be turned on until the voltage drop across the low-side MOSFET falls below the current limit threshold.

Choose a current limit setting resistor via the following equation :

$$R_{LIMIT} = I_{LIMIT} \times R_{DS(ON)} \times 10 / 5\mu A$$

And then the CS pin voltage is

$$V_{CS} = R_{LIMIT} \times 5\mu A$$

Note that the V_{CS} should be set from 0.4V to 3V.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by PHASE and PGND.

Current Protection for VTT

The LDO has an internally fixed constant over-current limit of 2.6A while operating at normal condition. From then on, when the output voltage exceeds 20% of its set voltage, the internal power good signal will transit from high to low.

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the VDD supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins.

A dead-time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

The low-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor that drives LGATE low is robust, with a 0.8Ω typical on-resistance. A 5V bias voltage is delivered from the VDD supply. The instantaneous drive current is supplied by the flying capacitor between VDD and PGND.

For high current applications, some combinations of high- and low-side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing shoot through currents. This is often remedied by adding a resistor in series on BOOT, which increases the turn-on rising time of the high-side MOSFET without degrading the turn-off time (Figure 5).

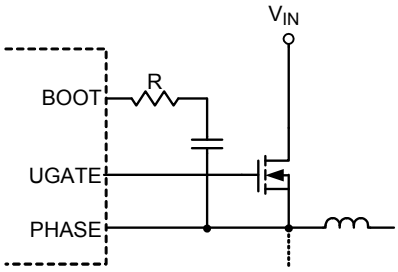


Figure 5. Increasing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open drain output that requires a pull-up resistor. When the output voltage is 15% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to 87% of its set voltage once more. During soft-start, PGOOD is actively held low and only allowed to be pulled high after soft-start is over and the output reaches 87% of its set voltage. There is a 5μs delay built into PGOOD circuitry to prevent false transition.

POR Protection

The RT8248A has a VDD supply power on reset protection (POR). When the VDD voltage is higher than 4.2V (typ.), VDDQ, VTT and VTTREF will be activated. This is a non-latch protection.

Soft-Start

The RT8248A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. Soft-start (SS) automatically begins once the chip is enabled. During soft-start, internal bandgap circuit gradually ramps up the reference voltage from zero. The maximum reference value is set externally as described in Table 1.

The soft-start function of VTT is achieved by the current limit and VTTREF voltage through the internal RC delay ramp up after S3 is high. During VTT startup, the current limit level is 2.6A. This allows the output to start up smoothly and safely under enough source/sink ability.

Output Over-Voltage Protection (OVP)

The output voltage can be continuously monitored for over-voltage condition. If the output exceeds 15% of its set voltage threshold, over voltage protection will be triggered

and the LGATE low-side gate driver will be forced high. This activates the low-side MOSFET switch which rapidly discharges the output capacitor and reduces the output voltage. There is a 5µs latch delay built into the over-voltage protection circuit. The RT8248A will be latched if the output voltage remains above the OV threshold after the latch delay period. The latched OVP will pull low PGOOD and can only be released by VDD power on reset or S5.

Note that latching the LGATE high will cause the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over voltage condition is caused by a shorted high-side switch, turning the low-side MOSFET on 100% will create an electrical shorted circuit between the battery and GND, to blow the fuse and disconnecting the battery from the output.

Output Under-Voltage Protection (UVP)

The output voltage can be continuously monitored for under-voltage condition. When UVP is enabled, the under voltage protection is triggered if the FB is less than 0.45V. Then, both UGATE and LGATE gate drivers will be forced low until next VDD or S5 reset. During soft-start, the UVP has a blanking time around 5ms.

Thermal Protection

The RT8248A features a thermal protection function. If the temperature exceeds the threshold, 165°C (typ.), the PWM output, VTTREF and VTT will be shut down. The RT8248A is latched once thermal shutdown is triggered and can only be released by VDD power on reset or S5.

Output Voltage Setting (FB)

Connect a resistive voltage divider at FB between VDDQ and GND to adjust the respective output voltage between 0.675V and 3.3V (Figure 6). Choose R2 to be approximately 10kΩ and solve for R1 using the equation as follows :

$$V_{VDDQ\ (Valley)} = V_{REF} \times \left(1+\left(\frac{R1}{R2}\right)\right)$$

where V_{REF} is 0.75V or 0.675V depends on the VID setting in Table 1.

Note that when the RT8248A operates from CCM to DEM, the reference voltage will add 10mV offset.

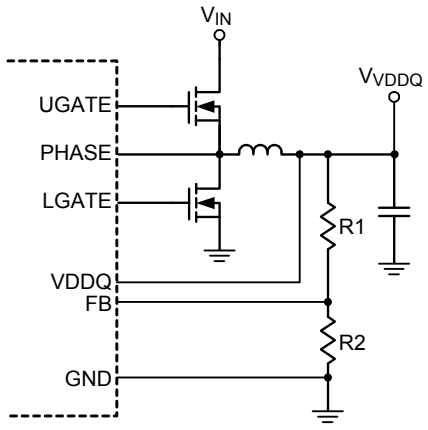


Figure 6. Setting VDDQ with a Resistive Voltage Divider

Table 1. VID and Reference Voltage Setting

VID	Reference Voltage (V)
High	0.675
Low	0.75

When the reference voltage is changed from 0.75V to 0.675V, the OVP latch will be masked for 120µs to prevent an unexpected shutdown.

VTT Linear Regulator and VTTREF

The RT8248A integrates a high performance low dropout linear regulator that is capable of sourcing and sinking currents up to 1.5A. This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough for keeping track of VTTREF within 40mV at all conditions, including fast load transient. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the VTT pin. For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 10µF. It is recommended to attach two 10µF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If ESR of the output capacitor is greater than 2mΩ, insert an RC filter between the output and VTTSNS input to achieve loop stability. The RC filter time constant should be almost the same or slightly lower than the time constant made

by the output capacitor and its ESR. The VTTREF block consists of on-chip 1/2 divider, LPF and buffer. This regulator also has sink and source capability up to 10mA. Bypass VTTREF to GND with a 33nF ceramic capacitor for stable operation.

Output Management by S3, S5 Control

In DDR2/DDR3 memory applications, it is important to always keep VDDQ higher than VTT/VTTREF, even during start-up and shutdown. The RT8248A provides this management by simply connecting both S3 and S5 terminals to the sleep-mode signals such as SLP_S3 and SLP_S5 in notebook PC system. All VDDQ, VTTREF and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance (high-Z) state. The VTT output is floated and does not sink or source current in this state. In S4/S5 states (S3 = S5 = low), all of the three outputs are disabled and discharged to ground. The code of each state represents the following: S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 2)

Table 2. S3 and S5 Truth Table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

VDDQ and VTT Discharge Mode

The RT8248A discharges VDDQ, VTTREF and VTT outputs when S5 is low or in the S4/S5 state.

When in non-tracking discharge mode, the RT8248A discharges outputs using internal MOSFETs which are connected to VDDQ and VTT. The current capability of these MOSFETs is limited to discharge slowly. Note that the VDDQ discharge current flows from VDDQ to GND in this mode. In order to discharge smoothly, the RT8248A provides a special function that the low-side MOSFET will switch periodically as phase pin with remaining voltage.

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or L_{IR}) determine the inductor value as follows :

$$L = \frac{t_{ON} \times (V_{IN} - V_{VDDQ})}{L_{IR} \times I_{LOAD(MAX)}}$$

where L_{IR} is the ratio of the peak-to-peak ripple current to the maximum average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left[(L_{IR}/2) \times I_{LOAD(MAX)} \right]$$

This inductor ripple current also impacts transient-response performance, especially at low $V_{IN} - V_{VDDQ}$ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the output transient. V_{SAG} also features a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{VDDQ} \times (t_{ON} + t_{OFF(MIN)}) \right]}$$

where minimum off-time, $t_{OFF(MIN)}$, is 400ns typically.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak-to-peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} = \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{VDDQ}}$$

where I_{PEAK} is the peak inductor current.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-20L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 7 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

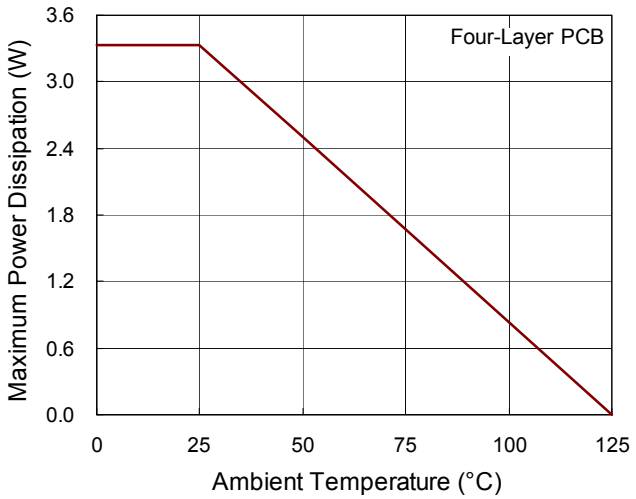


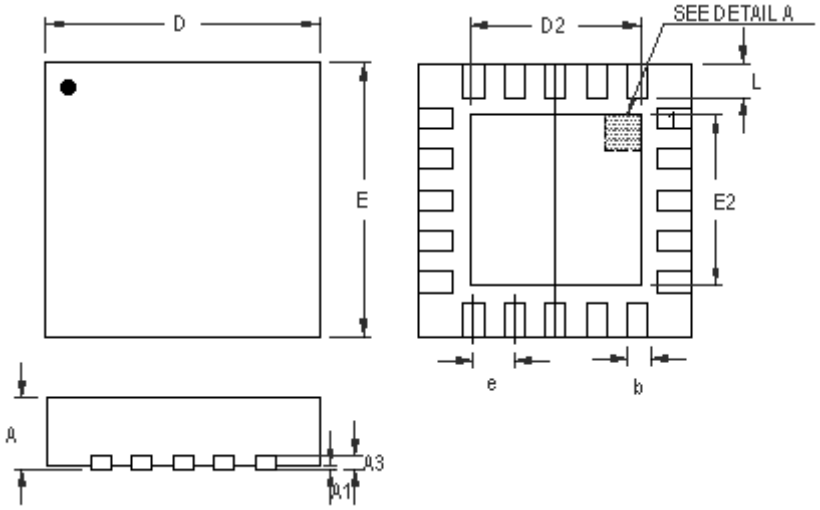
Figure 7. Derating Curve of Maximum Power Dissipation

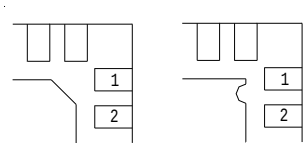
Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for the RT8248A.

- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VDDQ, FB, PGND, PGOOD, CS, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, and BOOT to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed as close as possible to the pin with short and wide trace.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- It is strongly recommended to connect VTTSNS to the positive node of VTT output capacitor(s) as a separate trace from the high current power line to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. It is also recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor(s).
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed as close to the IC as possible to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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