PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8734
Dated 17 Oct 2014

PDIP7 and SDIP10 VIPER products: assembling and testing transfer from ST LONGGANG to NANTONG FUJITSU subcon and to ST MUAR

Table 1. Change Implementation Schedule

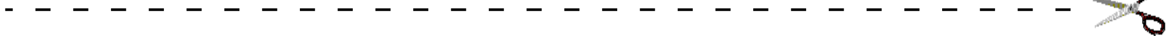
Forecasted implementation date for change	20-Nov-2014
Forecasted availability date of samples for customer	15-Nov-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Dec-2014
Estimated date of changed product first shipment	16-Jan-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Package assembly location change, Testing location change
Reason for change	Our internal LGG facility is proceeding in a shut down road map.
Description of the change	ST is pursuing the plan to rationalize the manufacturing processes. Because of this, ST is announcing the transfer ot assembling and testing activities originally installed in our Longgang (LGG) facility in China to Nantong Fujitsu (NFME) subcon facility in China. All testing activities originally performed in LGG will be transferred to ST Muar-Malaysia facility. The transfer will impact on all packages families actually present in LGG. More specifically the different PDIP package families will be transferred to the NFME subcon facility. Implementation will occur all along the year, till end of 2014. Packages will be transferred in sequence and depending on Test Vehicles, implemented and released at different time frames within the year.
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8734**
Please sign and return to STMicroelectronics Sales Office	**Dated 17 Oct 2014**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Sandrini, Francesca Marta	Marketing Manager
Borghi, Maria Rosa	Product Manager
Moretti, Paolo	Q.A. Manager

PDIP7 AND SDIP10 VIPER PRODUCTS: ASSEMBLING AND TESTING TRANSFER FROM ST- LONGGANG TO NANTONG FUJITSU SUBCON AND ST-MUAR

WHAT is the change?

ST is pursuing the plan to rationalize the manufacturing processes. Because of this, ST is announcing the transfer of assembling and testing activities originally installed in our Longgang (LGG) facility in China to Nantong Fujitsu (NFME) subcon facility in China. Majority of the testing activities originally performed in LGG will be transferred to ST Muar-Malaysia facility.
The transfer will impact on all packages families actually present in LGG. More specifically the different PDIP package families will be transferred to the NFME subcon facility. Implementation will occur all along the year, till end of 2014 and for some packages initial quarter 2015. Packages will be transferred in sequence and depending on Test Vehicles, implemented and released at different time frames.
The transfer will also imply in several cases material changes in view of rationalization. These changes are reported in more details within the PCN.

Present PCN is focused on PDIP7 and SDIP10 assembling and testing transfer. PCNs for PDIP14/16 and PDIP8 have been already issued and implementation is ongoing. Because of the nature of transfer, sample availability, qualification reports and initial shipping will occur not simultaneously but along a period of time. Estimated time frames are reported within the PCN.

Package	Impacted Product families	Change of Bill of Material (BOM) compared with previous BOM	FINAL TESTING SITE /TESTING PLATFORM CHANGE	
PDIP7 Assy and testing transfer to NFME and ST-Muar	Power Conversion – Dual Die Viper products	New BOM including molding compound and glue	Muar Testing site/No testing platform change	
SDIP10 Assy and testing transfer to NFME and ST-Muar	Power Conversion – Dual Die Viper products	New BOM including molding compound and glue	Muar Testing site/No testing platform change	

WHY:

Our internal LGG facility is proceeding in a shutdown road map. Therefore the related activities will be transferred to other facilities: NFME in Nantong –China (for assembling) and ST- Muar-Malaysia (for final testing).

WHEN will this change occur?

Package	Test vehicles by Commercial Products/Line codes	Test Vehicles Samples availability	Qualification Report availability (upon request)	Estimated First Shipment start date
PDIP7(*)	VIPER16-MV61	WK48	Final Report WK50	From WK52
	VIPER17-MV34	WK48	Final Report WK50	From WK52
SDIP10 (**)	VIPER37-MT19	WK52	Final Report WK05	From WK09

- (*) Preliminary Reports for the Test Vehicles are attached at this PCN
- (**) Qualification Plan for SDIP10 is attached

HOW will the change be qualified?

- New BOMs and Transfer activities have been evaluated by using the two most representatives products as Test Vehicles: VIPER16 and VIPER17 for PDIP7 and VIPER37 for SDIP10
- Results obtained by these TVs will be extended from reliability point of view to all the others PDIP7 and SDIP10 VIPER products.
- This change will be qualified using the standard STMicroelectronics procedures for quality and reliability.
  Major steps of the qualification are:
  - Process capability assessment and Workability on all TVs
  - DOE and Corner Lots
  - Reliability Trials on all TVs
  - Final Test Correlation

- Depending on TVs all or subset of the above qualification steps criteria will be applied

Test Vehicles	Workability	DOE Corner Lots	Final test Data and Correlation	Reliability Trial
VIPER16-MV61	X	X	X	X
VIPER17-MV34	X	X	X	X
VIPER37-MT19	X	X	X	X

IMPACTS OF THE CHANGE:

Form: No change
Fit: No change
Function: No change

APPENDICES:

- APPENDIX 1 Reliability qualification plan for involved Test Vehicles
- APPENDIX 2 Assy transfer to NFME and Testing transfer to Muar: List of Impacted commercial products

ATTACHMENTS:

- **Preliminary Reliability Report on VIPER16**
- **Preliminary Reliability Report on VIPER17**

APPENDIX 1: RELIABILITY QUALIFICATION PLAN

Test Vehicles by CP/Line codes	HTOL/HTRB (1000 hrs)	TEMPERATURE HUMIDITY BIAS (1000 hrs)	THERMAL CYCLES (1000 cy)	PRESSURE POT (96 hrs)	HIGH TEMPERATURE STORAGE (1000 hrs)
VIPER16-MV61	X	X	X	X	X
VIPER17-MV34 (*)	X	X	X	X	X
VIPER37-MT19	X	X	X	X	X

(*): ELFR stress test has been also performed on VIPER17 samples

Reliability Report

General Information	
Product Line	*MV61 (VL8Q+UP40)*
Product Description	*High Voltage Converter*
Product division	*I&PC*
Package	*PDIP7*
Silicon process technology	*BCD6 (UP40)* *SUPERMESH (VL8Q)*

Locations	
Wafer fab location	*ANG MO KIO (VL8Q)* *+ CATANIA (UP40)*
Assembly plant location	*NANTONG Fujitsu - CHINA*
Preliminary Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	10-Oct-12	9	S.Cannizzaro	Original document

Issued by

Salvatore Omar Cannizzaro

Approved by

Alceo Paratore

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation performed on MV61 (VL8Q+UP40) device diffused in ANG MO KIO (VL8Q) + CATANIA (UP40) and assembled in PDIP7 in NANTONG Fujitsu - CHINA, included in the overall plan of the transfer from Longgang assy plant to NFME-Fujitsu assy plant.

According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- High Temperature Reverse Bias

Package Oriented Tests

- Temperature Cycling
- Pressure Pot
- High Temperature Storage Life
- Temperature Humidity Bias

Electrical Characterization

- ESD resistance test

2.2 Conclusion

Taking in account the positive results of the trials performed on the MV61 (VL8Q+UP40) diffused in ANG MO KIO (VL8Q) + CATANIA (UP40) and assembled in PDIP7 in NANTONG Fujitsu - CHINA, a positive judgment can be given out.

2.3 Traceability

Wafer fab information UP40	
Wafer fab manufacturing location	*CATANIA*
Wafer diameter	*8 inches*
Wafer thickness	*375µm*
Silicon process technology	*BCD6 3M*
Die finishing back side	*RAW SILICON*
Die size	*1320x1112µm*
Bond pad metallization layers	*AlCu*
Passivation	*Polymide*
Metal levels	*3*

Wafer fab information VL8Q	
Wafer fab manufacturing location	*AMJ9*
Wafer diameter	*6 inches*
Wafer thickness	*280µm*
Silicon process technology	*SUPERMESH*
Die finishing back side	*Ti-Ni-Au*
Die size	*2650x1290µm*
Bond pad metallization layers	*AlSi*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*NANTONG Fujitsu - CHINA*
Package description	*PDIP7*
Molding compound	*8200DTA*
Wires bonding materials/diameters	*Au/1mil*
Die attach material	*8390*

3 TESTS RESULTS SUMMARY

3.1 Test plan and results summary

Die Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
HTOL	High Temperature Operating Life (Dymamic)						
		Tj=150°C Vdrain=100V (Idrain=350mA) Vcc=self-supplied; half samples size.	**0/78**	**0/78**	**0/78**	**168h**	
			0/78	**(*)**	**(*)**	**500h**	
		Tj=150°C Vdrain=750V (Idrain=100mA) Vdd=22V; half samples size.	**(*)**	**(*)**	**(*)**	**1000h**	
HTRB	High Temperature Reverse Bias (Static)						
		Tj=150°C Vdrain=800V, Vdd=22V	**0/77**	**0/77**	**0/77**	**168h**	
			0/77	**0/77**	**0/77**	**500h**	
			0/77	**(*)**	**(*)**	**1000h**	

Package Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
THB	Temperature Humidity Bias (Static)						
		Ta=85°c/85%R.H. Vcc=22V, Vdrain=520V	**0/25**	**0/25**	**0/25**	**168h**	
			0/25	**(*)**	**(*)**	**500h**	
			(*)	**(*)**	**(*)**	**1000h**	
AC	Pressure Pot						
		121°C 2atm	**0/25**	**0/25**	**0/25**	**168h**	
TC	Temperature Cycling						
		Temp. range: -50/+150°C	**0/25**	**0/25**	**0/25**	**200cy**	
			0/25	**0/25**	**0/25**	**500cy**	
			(*)	**(*)**	**(*)**	**1000cy**	
HTSL	High Temperature Storage Life (No bias)						
	No Bias	**Tamb=150°C**	**0/25**	**0/25**	**0/25**	**168h**	
			0/25	**0/25**	**0/25**	**500h**	
			0/25	**(*)**	**(*)**	**1000h**	

Electrical Characterization Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			Lot 1	**Lot 2**	**Lot 3**		
ESD	Electro Static Discharge						
	Charge Device Model	**+/- 1.5KV**	**0/3**	**-**	**-**		

(*) = Trial running

4 TESTS DESCRIPTION & DETAILED RESULTS

4.1 Die oriented tests

4.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electro migration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

4.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing @ 168hrs @ Ta=25°C

5 PACKAGE ORIENTED TESTS

5.1.1 High Temperature Storage Life

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.1.2 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.1.3 Pressure Pot

The purpose of this test is to point out critical water entry path with consequent electrochemical and galvanic corrosion effects.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

5.1.4 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

6 ELECTRICAL CHARACTERIZATION TESTS

6.1.1 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Charge Device Model** JEDEC STANDARD JESD22-C101
  CDF-AEC-Q100-011

Reliability Report

General Information	
Product Line	*MV34 (VZ8Q+UL39)*
Product Description	*High Voltage Converter*
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Assembly plant location	*NANTONG Fujitsu - CHINA*
Preliminary Reliability assessment	*Pass*

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According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- High Temperature Reverse Bias
- Early Life Failure Rate

Package Oriented Tests

- Temperature Cycling
- Pressure Pot
- High Temperature Storage Life
- Temperature Humidity Bias

Electrical Characterization

- ESD resistance test

2.2 Conclusion

Taking in account the positive results of the trials performed on the MV34 (VZ8Q+UL39) diffused in ANG MO KIO (VZ8Q) + CATANIA (UL39) and assembled in PDIP7 in NANTONG Fujitsu - CHINA, a positive judgment can be given out.

3 TRACEABILITY

Wafer fab information UP40	
Wafer fab manufacturing location	*CATANIA*
Wafer diameter	*8 inches*
Wafer thickness	*375µm*
Silicon process technology	*BCD6 3M*
Die finishing back side	*RAW SILICON*
Die size	*1320x1112µm*
Bond pad metallization layers	*AlCu*
Passivation	*Polymide*
Metal levels	*3*

Wafer fab information VL8Q	
Wafer fab manufacturing location	*AMJ9*
Wafer diameter	*6 inches*
Wafer thickness	*280µm*
Silicon process technology	*SUPERMESH*
Die finishing back side	*Ti-Ni-Au*
Die size	*2650x1290µm*
Bond pad metallization layers	*AlSi*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*NANTONG Fujitsu - CHINA*
Package description	*PDIP7*
Molding compound	*8200DTA*
Wires bonding materials/diameters	*Au/1mil*
Die attach material	*8390*

4 TESTS RESULTS SUMMARY

4.1 Test plan and results summary

Die Oriented Tests

Test	Method	Conditions	Failure/SS Lot 1	Failure/SS Lot 2	Failure/SS Lot 3	Duration	Note
HTOL	High Temperature Operating Life (Dymamic)						
		Tj=150°C Vdrain=100V (Idrain=500mA) Vcc=22V; half samples size.	0/78	0/78	0/78	168h	
		Tj=150°C Vdrain=800V (Idrain=100mA) Vdd=18V; half samples size.	0/78	(*)	(*)	500h	
			(*)	(*)	(*)	1000h	
HTRB	High Temperature Reverse Bias (Static)						
		Tj=150°C Vdrain=800V, Vdd=22V.	0/77	0/77	0/77	168h	
			(*)	(*)	(*)	500h	
			(*)	(*)	(*)	1000h	
ELFR	Early Life Failure Rate (Static)						
		Tj=150°C Vdrain=800V, Vdd=22V	0/800	0/800	0/800	48h	

Package Oriented Tests

Test	Method	Conditions	Failure/SS Lot 1	Failure/SS Lot 2	Failure/SS Lot 3	Duration	Note
THB	Temperature Humidity Bias (Static)						
		Ta=85°c/85%R.H. Vcc=22V, Vdrain=520V	0/25	0/25	0/25	168h	
			0/25	(*)	(*)	500h	
			(*)	(*)	(*)	1000h	
AC	Pressure Pot						
		121°C 2atm	0/25	0/25	0/25	168h	
TC	Temperature Cycling						
		Temp. range: -50/+150°C	0/25	0/25	0/25	200cy	
			0/25	0/25	0/25	500cy	
			(*)	(*)	(*)	1000cy	
HTSL	High Temperature Storage Life (No bias)						
	No Bias	Tamb=150°C	0/25	0/25	0/25	200h	
			0/25	0/25	0/25	500h	
			0/25	(*)	(*)	1000h	

Electrical Characterization Tests

Test	Method	Conditions	Failure/SS Lot 1	Failure/SS Lot 2	Failure/SS Lot 3	Duration	Note
ESD	Electro Static Discharge						
	Charge Device Model	+/- 1.5KV	0/3	-	-		

(*) = Trial running

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electro migration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing @ 168hrs @ Ta=25°C

5.1.3 Early Life Failure Rate

This test is to evaluate the defects inducing failure in early life.
The device is biased in static conditions at the max junction temperature.

The read-outs flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing (24 hr.) @ Ta=25°C

6 PACKAGE ORIENTED TESTS

6.1.1 High Temperature Storage Life

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

6.1.2 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

6.1.3 Pressure Pot

The purpose of this test is to point out critical water entry path with consequent electrochemical and galvanic corrosion effects.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

6.1.4 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

7 ELECTRICAL CHARACTERIZATION TESTS

7.1.1 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Charge Device Model** JEDEC STANDARD JESD22-C101
  CDF-AEC-Q100-011

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