dsPIC33F
Product Overview

dsPIC® DSC High-Performance 16-Bit Digital Signal Controllers

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dsPIC33F High-Performance 16-Bit Digital Signal Controller Product Overview

Operating Range

- DC – 40 MIPS (40 MIPS @ 3.0-3.6V, -40° to +85°C)
- Industrial temperature range (-40° to +85°C)

High-Performance DSC CPU

- Modified Harvard architecture
- C compiler optimized instruction set
- 16-bit wide data path
- 24-bit wide instructions
- Linear program memory addressing up to 4M instruction words
- Linear data memory addressing up to 64 Kbytes
- 84 base instructions: mostly 1 word/1 cycle
- Sixteen 16-bit general purpose registers
- Two 40-bit accumulators:
  - With rounding and saturation options
- Flexible and powerful addressing modes:
  - Indirect, modulo and bit-reversed
- Software stack
- 16 x 16 fractional/integer multiply operations
- 32/16 and 16/16 divide operations
- Single-cycle multiply-and-accumulate:
  - Accumulator write back for DSP operations
  - Dual data fetch
- Up to +/- 16-bit shifts, for up to 40-bit data

Direct Memory Access (DMA)

- 8-channel hardware DMA
- Allows data transfer between RAM and a peripheral while CPU is executing code (no cycle stealing)
- 2 KB of dual-ported DMA buffer area (DMA RAM) to store data transferred via DMA
- Most peripherals support DMA

Interrupt Controller

- 5-cycle latency
- 117 interrupt vectors
- Up to 67 available interrupt sources, up to 5 external interrupts
- 7 programmable priority levels
- 5 processor exceptions

Digital I/O

- Up to 85 programmable digital I/O pins
- Wake-up/Interrupt-on-Change on up to 24 pins
- Output pins can drive from 3.0V to 3.6V
- All digital input pins are 5V tolerant
- 4 mA sink and source on all I/O pins

On-Chip Flash and SRAM

- Flash program memory, up to 256 Kbytes
- Data SRAM (up to 30 Kbytes):
  - Includes 2 KB of DMA RAM

System Management

- Flexible clock options:
  - External, crystal, resonator, internal RC
  - Fully integrated PLL
  - Extremely low jitter PLL
- Power-up timer
- Oscillator Start-up Timer/Stabilizer
- Watchdog timer with its own RC oscillator
- Fail-Safe Clock Monitor
- Reset by multiple sources

Power Management

- On-chip 2.5V voltage regulator
- Switch between clock sources in real time
- Idle, Sleep and Doze modes with fast wake-up

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Timers/Capture/Compare/PWM

- Timer/Counters: up to nine 16-bit timers:
  - Can pair up to make four 32-bit timers
  - 1 timer runs as Real-Time Clock with external 32 kHz oscillator
  - Programmable prescaler
- Input Capture (up to 8 channels):
  - Capture on up, down or both edges
  - 16-bit capture input functions
  - 4-deep FIFO on each capture
- Output Compare (up to 8 channels):
  - Single or Dual 16-Bit Compare mode
  - 16-Bit Glitchless PWM mode

Communication Modules

- 3-wire SPI™ (up to 2 modules):
  - Framing supports I/O interface to simple codecs
  - Supports 8-bit and 16-bit data
  - Supports all serial clock formats and sampling modes
  - 8-word FIFO buffers
- I^2C™ (up to 2 modules):
  - Full Multi-Master Slave mode support
  - 7-bit and 10-bit addressing
  - Bus collision detection and arbitration
  - Integrated signal conditioning
  - Address masking
- UART (up to 2 modules):
  - Interrupt-on-address bit detect
  - Wake-up-on-Start bit from Sleep mode
  - 4-character TX and RX FIFO buffers
  - LIN bus support
  - IrDA® encoding and decoding in hardware
  - High-Speed Baud mode
- Data Conversion Interface (DCI) module:
  - Codec interface
  - Supports I^2S and AC'97 protocols
  - Up to 16-bit data words, up to 16 words per frame
  - 4-word deep TX and RX buffers
- Enhanced CAN 2.0B active (up to 2 modules):
  - Up to 8 transmit and up to 16 receive buffers
  - 16 receive filters and 3 masks
  - Loopback, Listen Only and Listen All Messages modes for diagnostics and bus monitoring
  - Wake-up on CAN message
  - FIFO mode using DMA

Motor Control Peripherals

- Motor Control PWM (up to 8 channels):
  - 4 duty cycle generators
  - Independent or Complementary mode
  - Programmable dead time and output polarity
  - Edge or center-aligned
  - Manual output override control
  - Up to 2 Fault inputs
  - Trigger for A/D conversions
  - PWM frequency for 16-bit resolution (@ 40 MIPS) = 1220 Hz for Edge-Aligned mode, 610 Hz for Center-Aligned mode
  - PWM frequency for 11-bit resolution (@ 40 MIPS) = 39.1 kHz for Edge-Aligned mode, 19.55 kHz for Center-Aligned mode
- Quadrature Encoder Interface module:
  - Phase A, Phase B and index pulse input
  - 16-bit up/down position counter
  - Count direction status
  - Position Measurement (x2 and x4) mode
  - Programmable digital noise filters on inputs
  - Alternate 16-bit Timer/Counter mode
  - Interrupt on position counter rollover/ underflow

Analog-to-Digital Converters

- Up to two 10-bit or 12-bit A/D modules in a device
- 10-bit 2.2 Msps or 12-bit 1 Msps conversion:
  - 2 or 4 simultaneous samples
  - Up to 32 input channels with auto-scanning
  - 16-deep result buffer
  - Conversion start can be manual or synchronized with 1 of 4 trigger sources
  - Conversion possible in Sleep mode
  - ±1 LSB max integral nonlinearity
  - ±1 LSB max differential nonlinearity

CMOS Flash Technology

- Low-power, high-speed Flash technology
- Fully static design
- 3.3V (+/- 10%) operating voltage
- Industrial temperature
- Low-power consumption

Packaging:

- 100-pin TQFP (14x14x1 mm and 12x12x1 mm)
- 80-pin TQFP (12x12x1 mm)
- 64-pin TQFP (10x10x1 mm)

Note:	See Table 1-1 and Table 1-2 for exact peripheral features per device.

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1.0 dsPIC33F PRODUCT FAMILIES

1.1 General Purpose Family

The dsPIC33F General Purpose Family (Table 1-1) is ideal for a wide variety of 16-bit MCU embedded applications. The variants with codec interfaces are well-suited for audio applications.

TABLE 1-1: dsPIC33F GENERAL PURPOSE FAMILY VARIANTS

Device	Pins	Program Flash Memory (KB)	RAM(1) (KB)	Timer 16-bit	Input Capture	Output Compare Std. PWM	Codec Interface	A/D Converter	UART	SPI™	I²C™	CAN	I/O Pins (Max)(2)	Packages
33FJ64GP206	64	64	8	9	8	8	1	1 A/D, 18 ch	2	2	1	0	53	PT
33FJ64GP306	64	64	16	9	8	8	1	1 A/D, 18 ch	2	2	2	0	53	PT
33FJ64GP310	100	64	16	9	8	8	1	1 A/D, 32 ch	2	2	2	0	85	PF, PT
33FJ64GP706	64	64	16	9	8	8	1	2 A/D, 18 ch	2	2	2	2	53	PT
33FJ64GP708	80	64	16	9	8	8	1	2 A/D, 24 ch	2	2	2	2	69	PT
33FJ64GP710	100	64	16	9	8	8	1	2 A/D, 32 ch	2	2	2	2	85	PF, PT
33FJ128GP206	64	128	8	9	8	8	1	1 A/D, 18 ch	2	2	1	0	53	PT
33FJ128GP306	64	128	16	9	8	8	1	1 A/D, 18 ch	2	2	2	0	53	PT
33FJ128GP310	100	128	16	9	8	8	1	1 A/D, 32 ch	2	2	2	0	85	PF, PT
33FJ128GP706	64	128	16	9	8	8	1	2 A/D, 18 ch	2	2	2	2	53	PT
33FJ128GP708	80	128	16	9	8	8	1	2 A/D, 24 ch	2	2	2	2	69	PT
33FJ128GP710	100	128	16	9	8	8	1	2 A/D, 32 ch	2	2	2	2	85	PF, PT
33FJ256GP506	64	256	16	9	8	8	1	1 A/D, 18 ch	2	2	2	1	53	PT
33FJ256GP510	100	256	16	9	8	8	1	1 A/D, 32 ch	2	2	2	1	85	PF, PT
33FJ256GP710	100	256	30	9	8	8	1	2 A/D, 32 ch	2	2	2	2	85	PF, PT

Note 1: RAM size is inclusive of 2 KB DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

1.2 Motor Control Family

This family of dsPIC33F controllers (Table 1-2) supports a variety of motor control applications, such as brushless DC motors, single and 3-phase induction motors and switched reluctance motors. These products are also well-suited for Uninterrupted Power Supply (UPS), inverters, Switched mode power supplies, power factor correction and also for controlling the power management module in servers, telecommunication equipment and other industrial equipment.

TABLE 1-2: dsPIC33F MOTOR CONTROL AND POWER CONVERSION FAMILY VARIANTS

Device	Pins	Program Flash Memory (KB)	RAM(1) (KB)	Timer 16-bit	Input Capture	Output Compare Std. PWM	Motor Control PWM	Quadrature Encoder Interface	Codec Interface	A/D Converter	UART	SPI™	I²C™	CAN	I/O Pins (Max)(2)	Packages
33FJ64MC506	64	64	8	9	8	8	8 ch	1	0	1 A/D, 16 ch	2	2	2	1	53	PT
33FJ64MC508	80	64	8	9	8	8	8 ch	1	0	1 A/D, 18 ch	2	2	2	1	69	PT
33FJ64MC510	100	64	8	9	8	8	8 ch	1	0	1 A/D, 24 ch	2	2	2	1	85	PF, PT
33FJ64MC706	64	64	16	9	8	8	8 ch	1	0	2 A/D, 16 ch	2	2	2	1	53	PT
33FJ64MC710	100	64	16	9	8	8	8 ch	1	0	2 A/D, 24 ch	2	2	2	2	85	PF, PT
33FJ128MC506	64	128	8	9	8	8	8 ch	1	0	1 A/D, 16 ch	2	2	2	1	53	PT
33FJ128MC510	100	128	8	9	8	8	8 ch	1	0	1 A/D, 24 ch	2	2	2	1	85	PF, PT
33FJ128MC706	64	128	16	9	8	8	8 ch	1	0	2 A/D, 16 ch	2	2	2	1	53	PT
33FJ128MC708	80	128	16	9	8	8	8 ch	1	0	2 A/D, 18 ch	2	2	2	1	69	PT
33FJ128MC710	100	128	16	9	8	8	8 ch	1	0	2 A/D, 24 ch	2	2	2	2	85	PF, PT
33FJ256MC510	100	256	16	9	8	8	8 ch	1	0	1 A/D, 24 ch	2	2	2	1	85	PF, PT
33FJ256MC710	100	256	30	9	8	8	8 ch	1	0	2 A/D, 24 ch	2	2	2	2	85	PF, PT

Note 1: RAM size is inclusive of 2 KB DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

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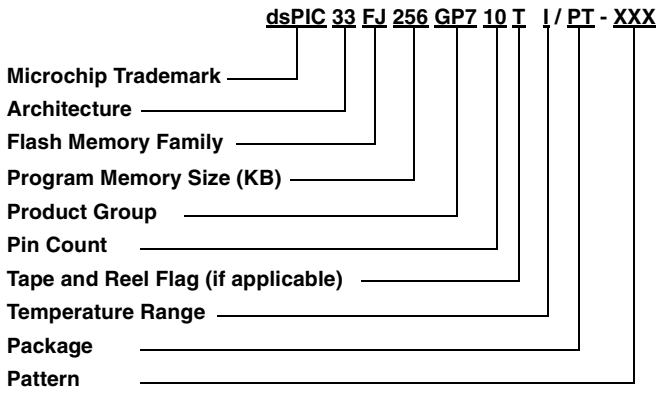
PRODUCT IDENTIFICATION SYSTEM



Architecture	33	=	16-bit Digital Signal Controller
Flash Memory Family	FJ	=	Flash program memory, 3.3V
Product Group	GP2	=	General Purpose family
	GP3	=	General Purpose family
	GP5	=	General Purpose family
	GP7	=	General Purpose family
	MC5	=	Motor Control family
	MC7	=	Motor Control family
Pin Count	06	=	64-pin
	08	=	80-pin
	10	=	100-pin
Temperature Range	I	=	-40°C to +85°C (Industrial)
Package	PT	=	10x10 or 12x12 mm TQFP (Thin Quad Flatpack)
	PF	=	14x14 mm TQFP (Thin Quad Flatpack)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)		
	ES	=	Engineering Sample

Examples:

a) dsPIC33FJ256GP710I/PT-PS:
General Purpose dsPIC33, 64 KB program memory, 100-pin, Industrial temp., TQFP package, Prototype Sample.

b) dsPIC33FJ64MC706I/PT-ES:
Motor Control dsPIC33, 64 KB program memory, 64-pin, Industrial temp., TQFP package, Engineering Sample.

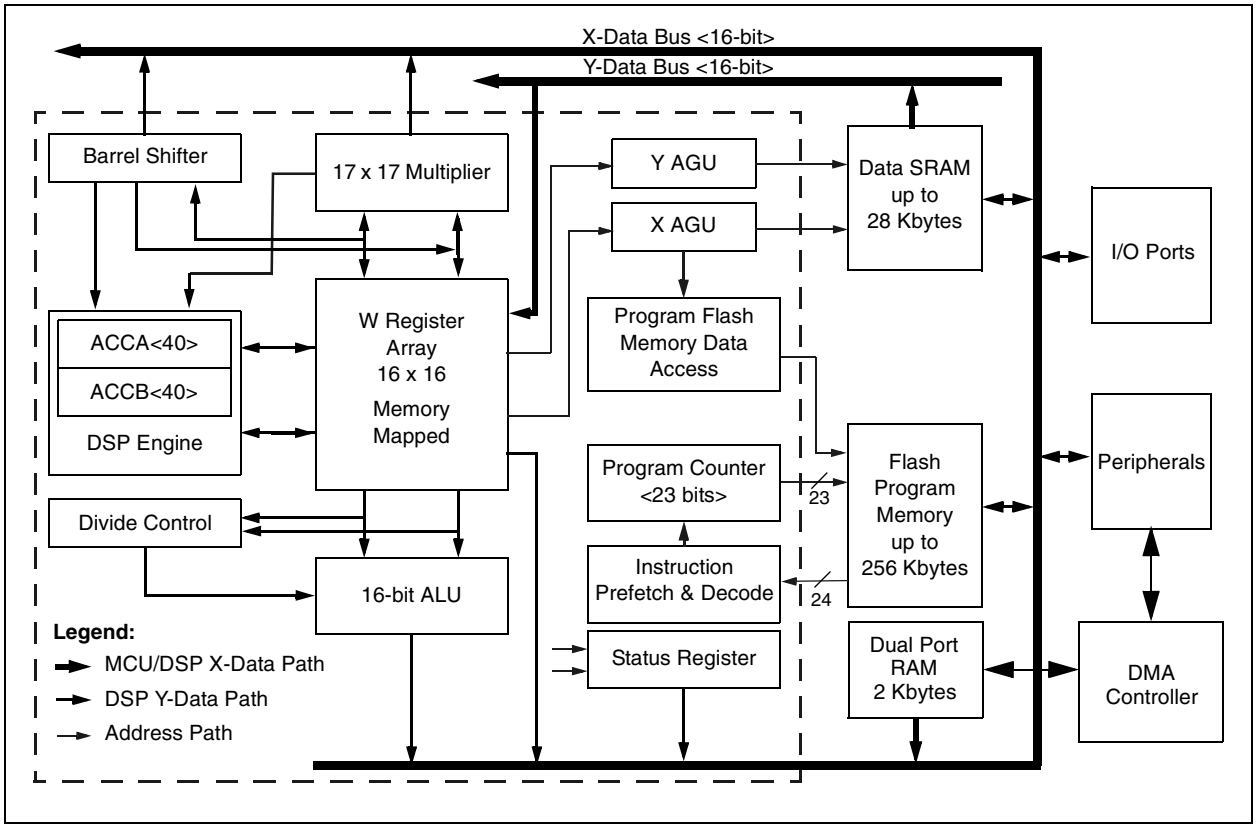
2.0 dsPIC33F DEVICE FAMILY OVERVIEW

The dsPIC33F device family employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together provide the dsPIC33F Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC33F devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use dsPIC33F devices.

Figure 2-1 shows a sample device block diagram typical of the dsPIC33F product family.

FIGURE 2-1: dsPIC33F DEVICE BLOCK DIAGRAM



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3.0 CPU ARCHITECTURE

3.1 Overview

The dsPIC33F CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented, as illustrated in Figure 3-1, varies from one device to another. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The dsPIC33F devices have sixteen 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33F instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency.

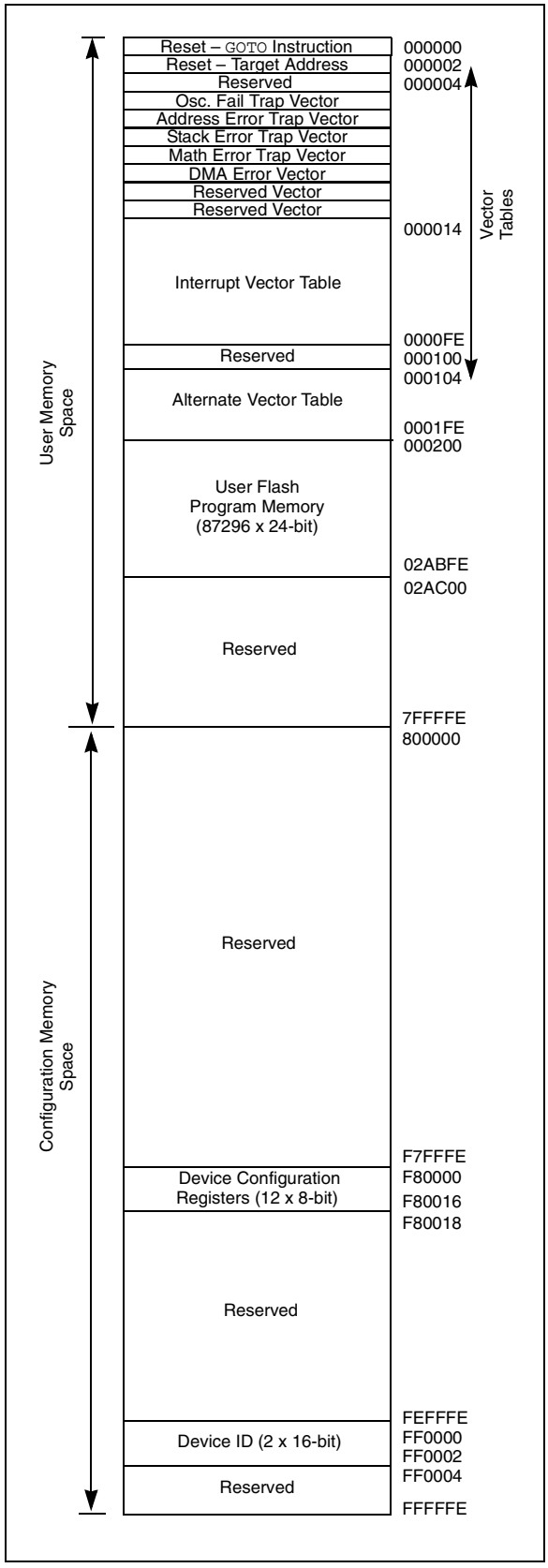
3.1.1 DATA MEMORY OVERVIEW

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device specific.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data space mapping feature lets any instruction access program space as if it were data space.

The data space includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

FIGURE 3-1: PROGRAM SPACE MEMORY MAP



3.1.2 ADDRESSING MODES OVERVIEW

Overhead-free circular buffers (modulo addressing) are supported in both X and Y address spaces. The modulo addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports bit-reversed addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The CPU supports Inherent (no operand), Relative, Literal, Memory Direct, Register Direct and Register Indirect Addressing modes. Each instruction is associated with a predefined addressing mode group depending upon its functional requirements. As many as 6 addressing modes are supported for each instruction.

For most instructions, the dsPIC33F is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

3.1.3 DSP ENGINE OVERVIEW

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value, up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The `MAC` instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

3.1.4 SPECIAL MCU FEATURES

The dsPIC33F features a 17-bit by 17-bit, single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed-sign multiplication, it also achieves accurate results for special operations such as (-1.0) x (-1.0).

The dsPIC33F supports 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

3.1.5 INTERRUPT OVERVIEW

The dsPIC33F has a vectored exception scheme with up to 5 sources of non-maskable traps and 67 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

3.1.6 FEATURES TO ENHANCE COMPILER EFFICIENCY

In addition to extensive DSP capability, the CPU architecture possesses several features that lead to a more efficient (code size and speed) C compiler.

1. For most instructions, three-parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.
2. Instruction addressing modes are extremely flexible to meet compiler needs.
3. The working register array consists of 16 x 16-bit registers, each of which can act as data, address or offset registers. One working register (W15) operates as the software Stack Pointer for interrupts and calls.
4. Linear indirect access of all data space is possible, plus the memory direct address range is up to 8 Kbytes. This capability, together with the addition of 16-bit direct address `MOV`-based instructions, has provided a contiguous linear addressing space.
5. Linear indirect access of 32K word (64 Kbyte) pages within program space is possible, using any working register via new table read and write instructions.
6. Part of data space can be mapped into program space, allowing constant data to be accessed as if it were in data space.

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3.2 Programmer's Model

The programmer's model, shown in Figure 3-2, consists of 16 x 16-bit working registers (W0 through W15), 2 x 40-bit accumulators (ACCA and ACCB), Status Register (SR), Data Table Page register (TBLPAG), Program Space Visibility Page register (PSVPAG), DO and REPEAT registers (DOSTART, DOEND, DCOUNT and RCOUNT) and Program Counter (PC). The working registers can act as data, address or offset registers. All registers are memory mapped. W0 is the W register for all instructions that perform file register addressing.

Some of these registers have a shadow register associated with them (see the legend in Figure 3-2). The shadow register is used as a temporary holding register and can transfer its contents to or from its host register upon some event occurring in a single cycle. None of the shadow registers are accessible directly.

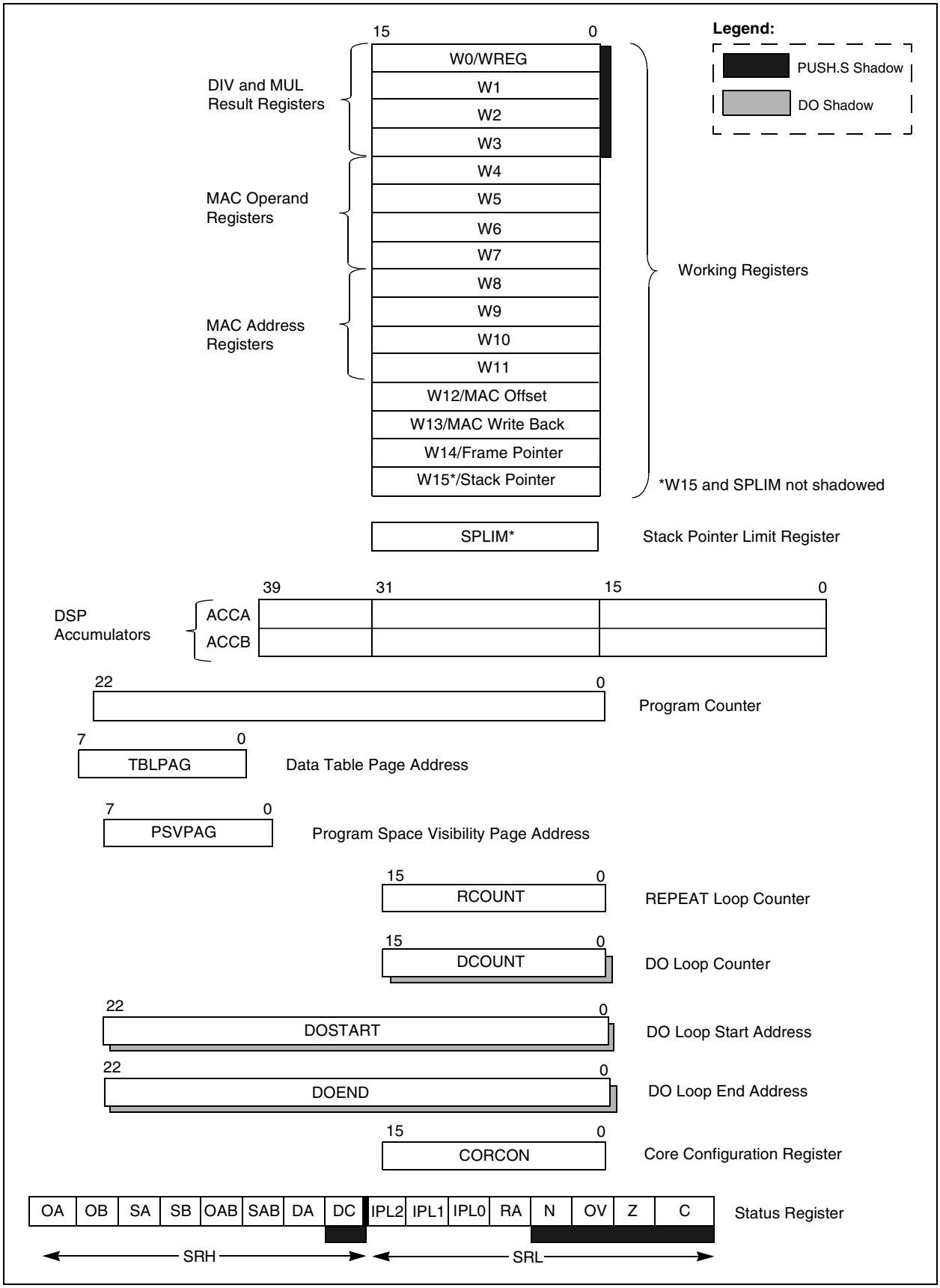
When a byte operation is performed on a working register, only the Least Significant Byte of the target register is affected. However, a benefit of memory mapped working registers is that both the Least and Most Significant Bytes can be manipulated through byte-wide data memory space accesses.

W15 is the dedicated software Stack Pointer (SP). It is automatically modified by exception processing and subroutine calls and returns. However, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies the reading, writing and manipulation of the Stack Pointer (e.g., creating stack frames).

W14 has been dedicated as a Stack Frame Pointer, as defined by the `LNK` and `ULNK` instructions. However, W14 can be referenced by any instruction in the same manner as all other W registers.

The Stack Pointer always points to the first available free word and grows from lower addresses towards higher addresses. It pre-decrements for stack pops (reads) and post-increments for stack pushes (writes).

FIGURE 3-2: PROGRAMMER'S MODEL



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3.3 Data Address Space

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

3.3.1 X AND Y DATA SPACES

The X data space is used by all instructions and supports all addressing modes. There are separate read and write data buses for X data space. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y data space is used in concert with the X data space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent (an example is shown in Figure 3-3) and is not user-programmable.

All effective addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes or 32K words, though the implemented memory locations vary from one device to another.

3.3.2 DMA RAM

Every dsPIC33F device contains 2 Kbytes of DMA RAM located at the end of Y data space. Memory locations in the DMA RAM space are accessible simultaneously by the CPU and the DMA Controller module. DMA RAM is utilized by the DMA Controller to store data to be transferred to various peripherals using DMA, as well as data transferred from various peripherals using DMA.

When the CPU and the DMA Controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

3.3.3 DATA SPACE WIDTH

The core data width is 16 bits. All internal registers are organized as 16-bit wide words. Data space memory is organized in byte addressable, 16-bit wide blocks. Figure 3-3 depicts a sample data space memory map for the dsPIC33F device with 33 Kbytes of RAM.

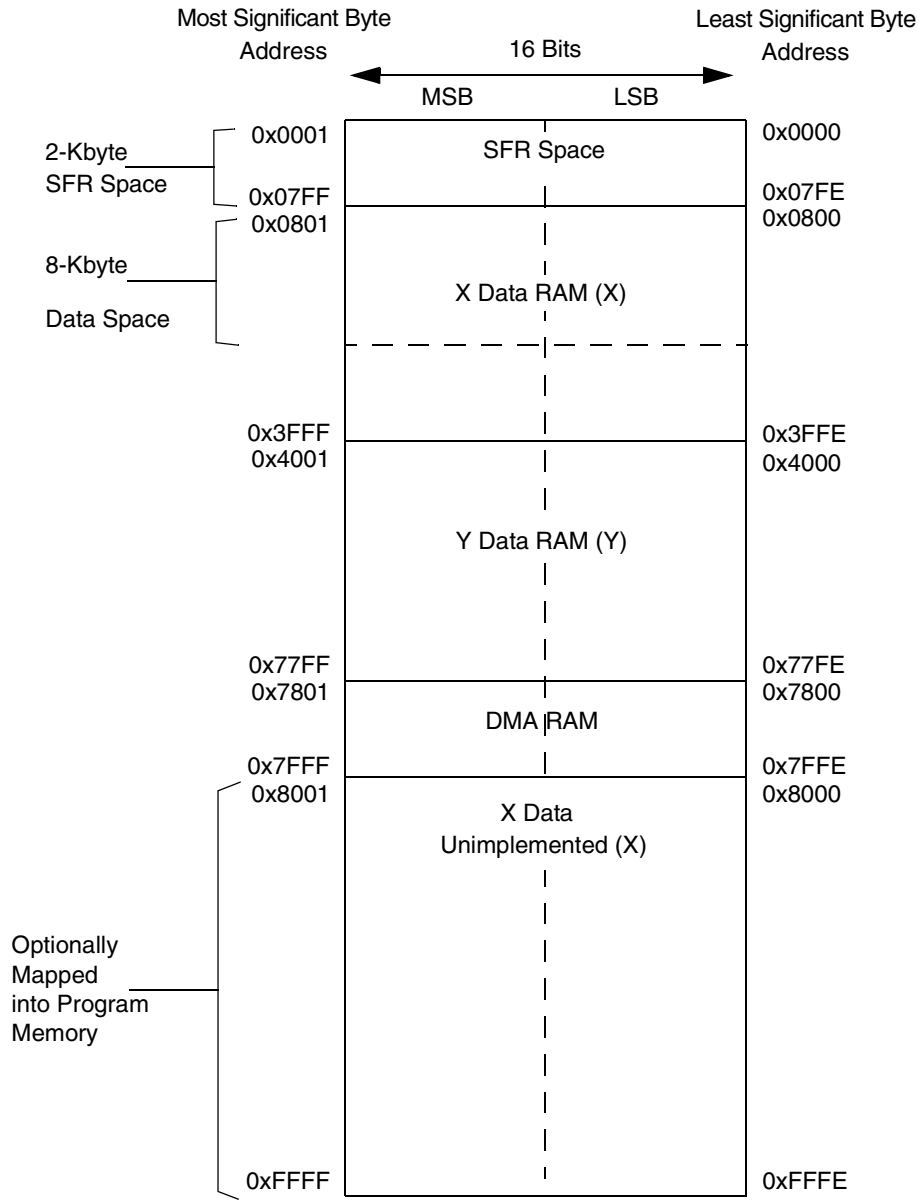
3.3.4 DATA ALIGNMENT

To help maintain backward compatibility with PICmicro® devices and improve data space memory usage efficiency, the dsPIC33F instruction set supports both word and byte operations. Data is aligned in data memory and registers as words, but all data space EAs resolve to bytes. Data byte reads will read the complete word which contains the byte, using the Least Significant bit (LSb) of any EA to determine which byte to select.

As a consequence of this byte accessibility, all effective address calculations are internally scaled. For example, the core would recognize that Post-Modified Register Indirect Addressing mode, [Ws++], will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported. Should a misaligned read or write be attempted, a trap will then be executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault.

FIGURE 3-3: SAMPLE DATA SPACE MEMORY MAP



Note: This data memory map is for the largest memory dsPIC33F device. Data memory maps for other devices may vary.

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3.4 DSP Engine

The DSP engine consists of a high-speed, single-cycle, 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtractor with two target accumulators, round and saturation logic, all of which enable efficient execution of computationally intensive DSP algorithms. The 17-bit x 17-bit multiplier is also utilized for MCU-based multiply instructions.

The DSP engine also has the capability to perform inherent accumulator-to-accumulator operations, which require no additional data. These instructions are `ADD`, `SUB` and `NEG`. This feature greatly simplifies basic arithmetic operations on 32-bit or 40-bit data.

A block diagram of the DSP engine is shown in Figure 3-4.

3.4.1 17 x 17-BIT MULTIPLIER

The 17 x 17-bit multiplier is capable of signed or unsigned operation. It can suitably scale its output to support either 1.31 fractional (Q31) or 32-bit integer results, thereby diminishing the need to manually post-process multiplication results for fractional data.

3.4.2 40-BIT ACCUMULATORS

The data accumulators have a 40-bit adder/subtractor with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the `ADD` and `LAC` instructions, the data to be accumulated or loaded can be optionally scaled via the barrel shifter prior to accumulation.

The adder/subtractor generates overflow status bits, SA/SB and OA/OB, which are latched and reflected in the Status register and can also optionally generate an arithmetic error trap:

- Overflow from bit 39. This is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39. This is a recoverable overflow. This bit (OA/OB) is set whenever all the guard bits are not identical to each other.

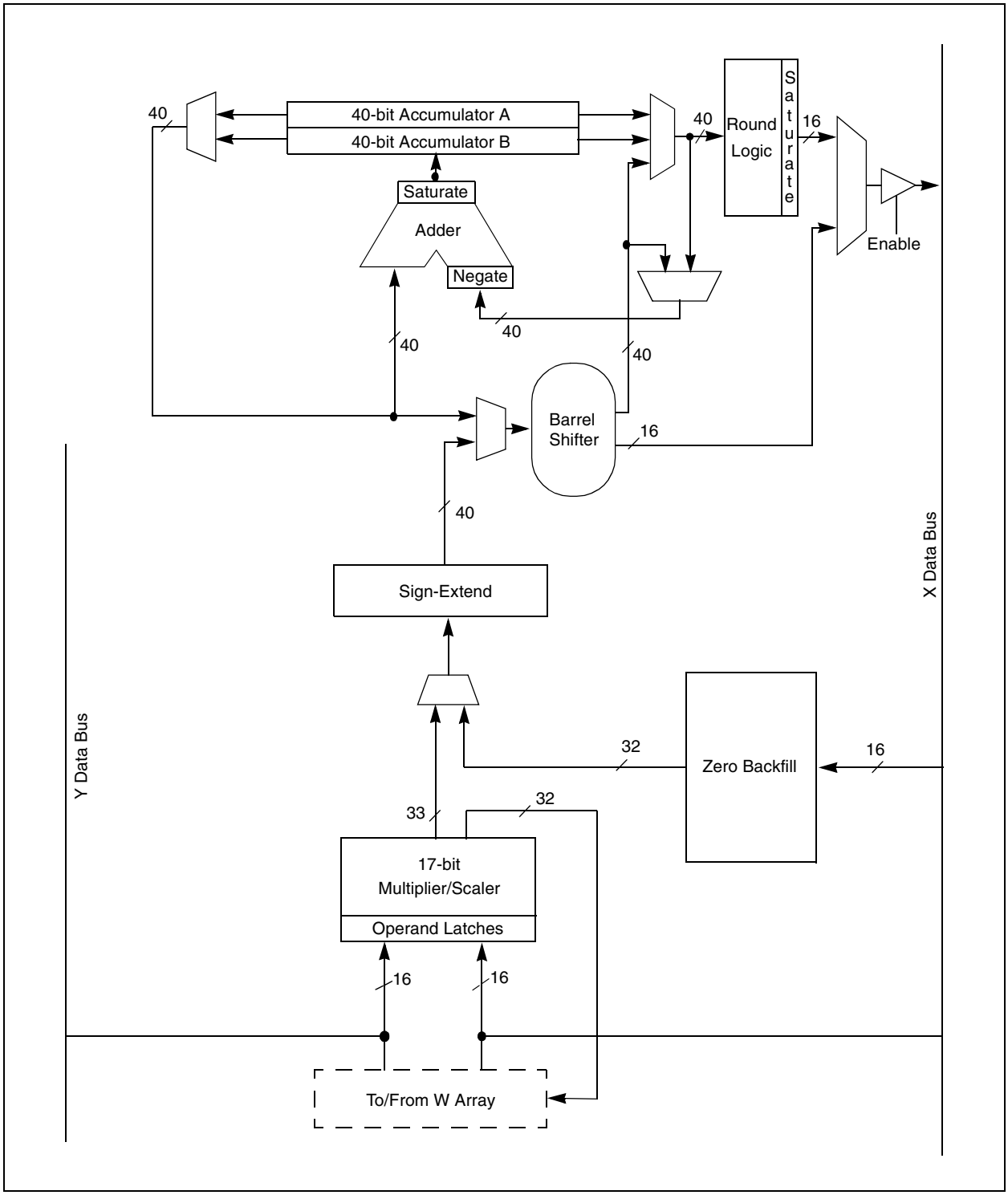
3.4.3 SATURATION AND OVERFLOW

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the overflow status bits described above and the user-configured control bits to determine when to saturate and to what value to saturate (a 40-bit or a 32-bit value).

In addition to adder/subtractor saturation, writes to data space can also be saturated, but without affecting the contents of the source accumulator.

The rounding logic performs a conventional (biased) or convergent (unbiased) data rounding function during an accumulator write (store). The Round mode is user-selectable. Rounding generates a 16-bit, 1.15 data value, which is passed to the data space write saturation logic. Data space write saturation ensures that the data in the accumulator is written back accurately even when rounding is performed. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

FIGURE 3-4: DSP ENGINE BLOCK DIAGRAM



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4.0 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a very efficient mechanism of copying data between peripheral SFRs (e.g., UART Receive register, Input Capture 1 buffer) and buffers or variables stored in RAM with minimal CPU intervention. The DMA Controller can automatically copy entire blocks of data, without the user software having to read or write peripheral Special Function Registers (SFRs) every time a peripheral interrupt occurs. To exploit the DMA capability, the corresponding user buffers or variables must be located in DMA RAM space.

The DMA Controller features eight identical data transfer channels, each with its own set of control and status registers. The UART, SPI, DCI, Input Capture, Output Compare, ECAN™ and A/D modules can utilize DMA. Each DMA channel can be configured to copy data either from buffers stored in DMA RAM to peripheral SFRs or from peripheral SFRs to buffers in DMA RAM.

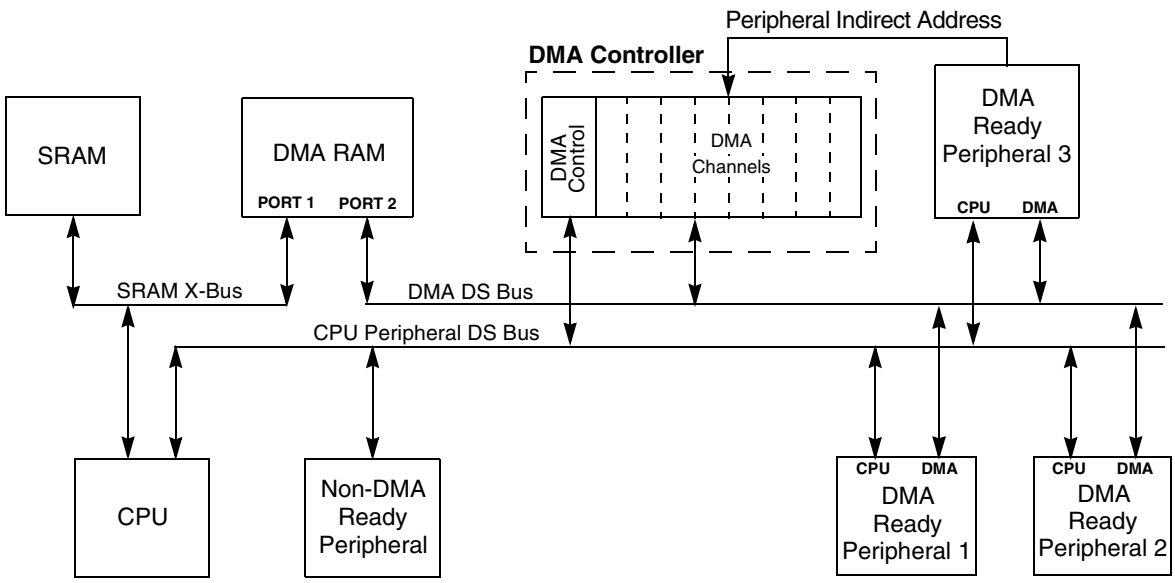
Each channel supports the following features:

- Word or byte-sized data transfers
- Transfers from peripheral to DMA RAM or DMA RAM to peripheral
- Indirect addressing of DMA RAM locations with or without automatic post-increment
- Peripheral Indirect Addressing – In some peripherals, the DMA RAM read/write addresses may be partially derived from the peripheral
- One-Shot Block Transfers – Terminating DMA transfer after one block transfer
- Continuous Block Transfers – Reloading DMA RAM buffer start address after every block transfer is complete
- Ping-Pong Mode – Switching between two DMA RAM start addresses between successive block transfers, thereby filling two buffers alternately
- Automatic or manual initiation of block transfers
- Each channel can select from 32 possible sources of data sources or destinations

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled. Additionally, a DMA error trap is generated in either of the following Fault conditions:

- DMA RAM data write collision between the CPU and a peripheral
- Peripheral SFR data write collision between the CPU and the DMA Controller

FIGURE 4-1: TOP LEVEL SYSTEM ARCHITECTURE USING A DEDICATED TRANSACTION BUS



Note: CPU and DMA address buses are not shown for clarity.

5.0 EXCEPTION PROCESSING

The dsPIC33F has four processor exceptions (traps) and up to 67 sources of interrupts, which must be arbitrated based on a priority scheme.

The processor core is responsible for reading the Interrupt Vector Table (IVT) and transferring the address contained in the interrupt vector to the program counter.

The Interrupt Vector Table (IVT) and Alternate Interrupt Vector Table (AIVT) are placed near the beginning of program memory (0x000004) for ease of debugging.

The interrupt controller hardware pre-processes the interrupts before they are presented to the CPU. The interrupts and traps are enabled, prioritized and controlled using centralized Special Function Registers.

Each individual interrupt source has its own vector address and can be individually enabled and prioritized in user software. Each interrupt source also has its own status flag. This independent control and monitoring of the interrupt eliminates the need to poll various status flags to determine the interrupt source

Table 5-1 contains information about the interrupt vector.

Certain interrupts have specialized control bits for features like edge or level triggered interrupts, interrupt-on-change, etc. Control of these features remains within the peripheral module, which generates the interrupt.

The special `DISI` instruction can be used to disable the processing of interrupts of priorities 6 and lower for a certain number of instruction cycles, during which the DISI bit remains set.

TABLE 5-1: INTERRUPT VECTORS

Vector Number	IVT Address	AIVT Address	Interrupt Source
8	0x000014	0x000114	INT0 – External Interrupt 0
9	0x000016	0x000116	IC1 – Input Compare 1
10	0x000018	0x000118	OC1 – Output Compare 1
11	0x00001A	0x00011A	T1 – Timer1
12	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	0x00001E	0x00011E	IC2 – Input Capture 2
14	0x000020	0x000120	OC2 – Output Compare 2
15	0x000022	0x000122	T2 – Timer2
16	0x000024	0x000124	T3 – Timer3
17	0x000026	0x000126	SPI1E – SPI1 Error
18	0x000028	0x000128	SPI1D – SPI1 Transfer Done
19	0x00002A	0x00012A	U1RX – UART1 Receiver
20	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	0x00002E	0x00012E	ADC1 – A/D Converter 1
22	0x000030	0x000130	DMA1 – DMA Channel 1
23	0x000032	0x000132	Reserved
24	0x000034	0x000134	I2C1D – I2C1 Transfer Done
25	0x000036	0x000136	I2C1E – I2C1 Bus Collision Error
26	0x000038	0x000138	Reserved
27	0x00003A	0x00013A	Change Notification Interrupt
28	0x00003C	0x00013C	INT1 – External Interrupt 1
29	0x00003E	0x00013E	ADC2 – A/D Converter 2
30	0x000040	0x000140	IC7 – Input Capture 7
31	0x000042	0x000142	IC8 – Input Capture 8
32	0x000044	0x000144	DMA2 – DMA Channel 2
33	0x000046	0x000146	OC3 – Output Compare 3
34	0x000048	0x000148	OC4 – Output Compare 4
35	0x00004A	0x00014A	T4 – Timer4
36	0x00004C	0x00014C	T5 – Timer5
37	0x00004E	0x00014E	INT2 – External Interrupt 2
38	0x000050	0x000150	U2RX – UART2 Receiver
39	0x000052	0x000152	U2TX – UART2 Transmitter

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TABLE 5-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	IVT Address	AIVT Address	Interrupt Source
40	0x000054	0x000154	SPI2E – SPI2 Error
41	0x000056	0x000156	SPI1D – SPI1 Transfer Done
42	0x000058	0x000158	C1RX – ECAN1 Receive Data Ready
43	0x00005A	0x00015A	C1 – CAN1 Event
44	0x00005C	0x00015C	DMA3 – DMA Channel 3
45	0x00005E	0x00015E	IC3 – Input Capture 3
46	0x000060	0x000160	IC4 – Input Capture 4
47	0x000062	0x000162	IC5 – Input Capture 5
48	0x000064	0x000164	IC6 – Input Capture 6
49	0x000066	0x000166	OC5 – Output Compare 5
50	0x000068	0x000168	OC6 – Output Compare 6
51	0x00006A	0x00016A	OC7 – Output Compare 7
52	0x00006C	0x00016C	OC8 – Output Compare 8
53	0x00006E	0x00016E	Reserved
54	0x000070	0x000170	DMA4 – DMA Channel 4
55	0x000072	0x000172	T6 – Timer6
56	0x000074	0x000174	T7 – Timer7
57	0x000076	0x000176	I2C2D – I2C2 Transfer Done
58	0x000078	0x000178	I2C2E – I2C2 Bus Collision Error
59	0x00007A	0x00017A	T8 – Timer8
60	0x00007C	0x00017C	T9 – Timer9
61	0x00007E	0x00017E	INT3 – External Interrupt 3
62	0x000080	0x000180	INT4 – External Interrupt 4
63	0x000082	0x000182	C2RX – ECAN2 Receive Data Ready
64	0x000084	0x000184	C2 – CAN2 Event
65	0x000086	0x000186	PWM – PWM Period Match
66	0x000088	0x000188	QEI – Position Counter Compare
67	0x00008A	0x00018A	DCIE – DCI Error
68	0x00008C	0x00018C	DCID – DCI Transfer Done
69	0x00008E	0x00018E	DMA5 – DMA Channel 5
70	0x000090	0x000190	RTC – Real-Time Clock
71	0x000092	0x000192	FLTA – MCPWM Fault A
72	0x000094	0x000194	FLTB – MCPWM Fault B
73	0x000096	0x000196	U1E – UART1 Error
74	0x000098	0x000198	U2E – UART2 Error
75	0x00009A	0x00019A	Reserved
76	0x00009C	0x00019C	DMA6 – DMA Channel 6
77	0x00009E	0x00019E	DMA7 – DMA Channel 7
78	0x0000A0	0x0001A0	C1TX – ECAN1 Transmit Data Request
			Reserved (for devices marked “PS”)
79	0x0000A2	0x0001A2	C2TX – ECAN2 Transmit Data Request
			Reserved (for devices marked “PS”)
80-125	0x0000A4-0x0000FE	0x0001A4-0x0001FE	Reserved

5.1 Interrupt Priority

Each interrupt source can be user-assigned to one of 8 priority levels, 0 through 7. Levels 7 and 1 represent the highest and lowest maskable priorities, respectively. A priority level of 0 disables the interrupt.

Since more than one interrupt request source may be assigned to a user-specified priority level, a means is provided to assign priority within a given level. This method is called “Natural Order Priority”.

The Natural Order Priority of an interrupt is numerically identical to its vector number. The Natural Order Priority scheme has 0 as the highest priority and 74 as the lowest priority.

The ability for the user to assign every interrupt to one of eight priority levels implies that the user can assign a very high overall priority level to an interrupt with a low Natural Order Priority, thereby providing much flexibility in designing applications that use a large number of peripherals.

5.2 Interrupt Nesting

Interrupts, by default, are nestable. Any ISR that is in progress may be interrupted by another source of interrupt with a higher user-assigned priority level. Interrupt nesting may be optionally disabled by setting the NSTDIS control bit (INTCON1<15>). When the NSTDIS control bit is set, all interrupts in progress will force the CPU priority to level 7 by setting IPL<2:0> = 111. This action will effectively mask all other sources of interrupt until a RETFIE instruction is executed. When interrupt nesting is disabled, the user-assigned interrupt priority levels will have no effect, except to resolve conflicts between simultaneous pending interrupts.

The IPL<2:0> bits become read-only when interrupt nesting is disabled. This prevents the user software from setting IPL<2:0> to a lower value, which would effectively re-enable interrupt nesting.

5.3 Traps

Traps can be considered as non-maskable, nestable interrupts that adhere to a fixed priority structure. Traps are intended to provide the user a means to correct erroneous operation during debug and when operating within the application. If the user does not intend to take corrective action in the event of a trap error condition, these vectors must be loaded with the address of a software routine that will reset the device. Otherwise, the trap vector is programmed with the address of a service routine that will correct the trap condition.

The dsPIC33F has four implemented sources of non-maskable traps:

- Oscillator Failure Trap
- Address Error Trap
- Stack Error Trap
- Math Error Trap
- DMA Trap

Many of these trap conditions can only be detected when they happen. Consequently, the instruction that caused the trap is allowed to complete before exception processing begins. Therefore, the user may have to correct the action of the instruction that caused the trap.

Each trap source has a fixed priority as defined by its position in the IVT. An oscillator failure trap has the highest priority, while an arithmetic error trap has the lowest priority.

Table 5-2 contains information about the trap vector.

5.4 Generating a Software Interrupt

Any available interrupt can be manually generated by user software (even if the corresponding peripheral is disabled), simply by enabling the interrupt and then setting the interrupt flag bit when required.

TABLE 5-2: TRAP VECTORS

Vector Number	IVT Address	AIVT Address	Trap Source
0	0x000004	0x000084	Reserved
1	0x000006	0x000086	Oscillator Failure
2	0x000008	0x000088	Address Error
3	0x00000A	0x00008A	Stack Error
4	0x00000C	0x00008C	Math Error
5	0x00000E	0x00008E	DMA Error Trap
6	0x000010	0x000090	Reserved
7	0x000012	0x000092	Reserved

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6.0 SYSTEM INTEGRATION

System management services provided by the dsPIC33F device family include:

- Control of clock options and oscillators
- Power-on Reset
- Oscillator Start-up Timer/Stabilizer
- Watchdog Timer with RC oscillator
- Fail-Safe Clock Monitor
- Reset by multiple sources

6.1 Clock Options and Oscillators

There are 7 clock options provided by the dsPIC33F:

- FRC Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- LPRC Oscillator

The FRC (Fast RC) internal oscillator runs at a nominal frequency of 7.37 MHz. The user software can tune the FRC frequency. User software can specify a factor by which this clock frequency is scaled.

The primary oscillator can use one of the following as its clock source:

1. XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
2. HS (High-Speed Crystal): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
3. EC (External Clock): External clock signal in the range of 0.8 MHz to 64 MHz. The external clock signal is directly applied to the OSC1 pin.

The secondary (LP) oscillator is designed for low power and uses a 32 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

The LPRC (Low-Power RC) internal oscIllator runs at a nominal frequency of 32.768 kHz. Another scaled reference clock is used by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase Locked Loop (PLL) to provide a wide range of output frequencies for device operation. The input to the PLL can be in the range of 1.6 MHz to 16 MHz, and the PLL Phase Detector Input Divider, PLL Multiplier Ratio and PLL Voltage Controlled Oscillator (VCO) can be individually configured by user software to generate output frequencies in the range of 25 MHz to 160 MHz.

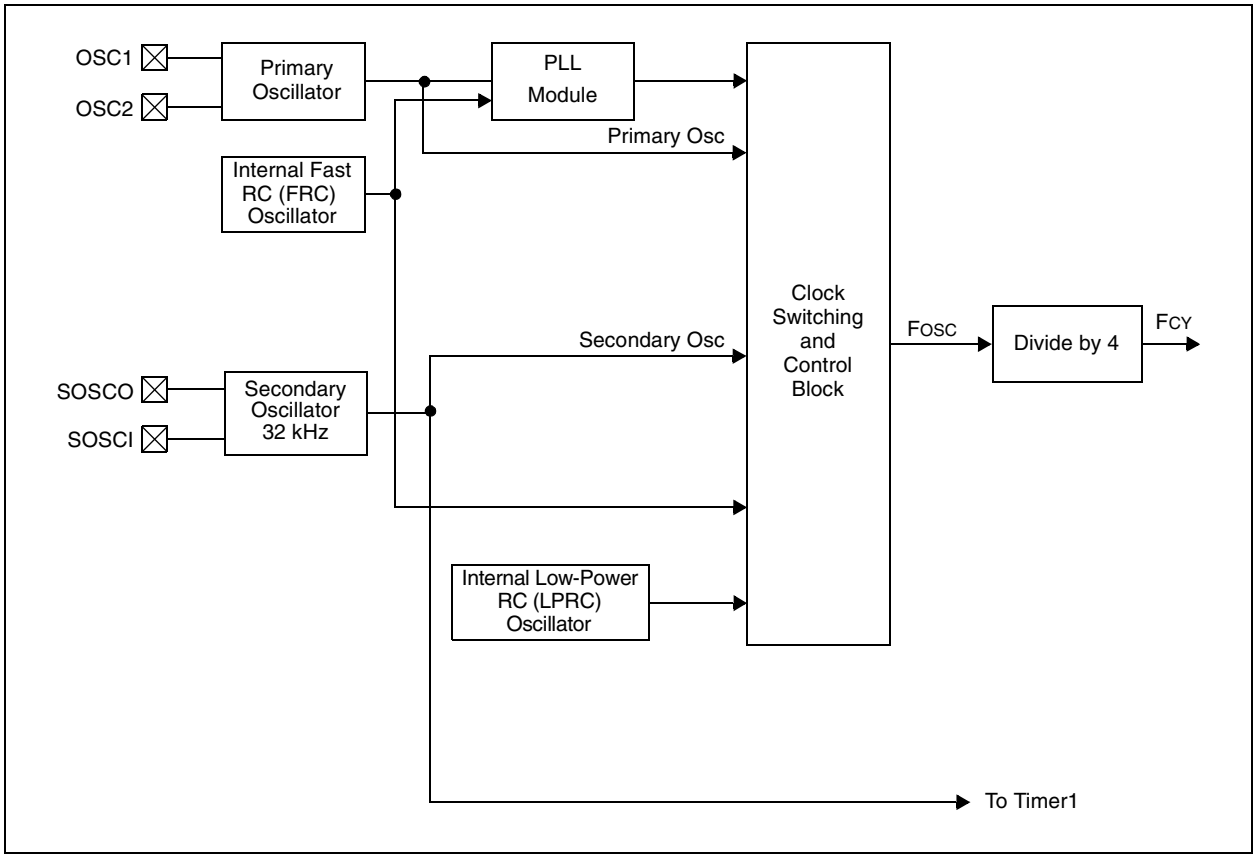
The output of the oscillator (or the output of the PLL if a PLL mode has been selected) is divided by 4 to generate the device instruction clock (FCY). FCY defines the operating speed of the device, and speeds up to 40 MHz are supported by the dsPIC33F architecture.

The dsPIC33F oscillator system provides:

- Various external and internal oscillator options as clock sources
- An on-chip PLL to scale the internal operating frequency to the required system clock frequency
- The internal FRC oscillator can also be used with the PLL, thereby allowing full-speed operation without any external clock generation hardware
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- A Clock Control register (OSCCON)
- Nonvolatile configuration bits for main oscillator selection.

A simplified block diagram of the oscillator system is shown in Figure 6-1.

FIGURE 6-1: OSCILLATOR SYSTEM BLOCK DIAGRAM



6.2 Power-on Reset

When a supply voltage is applied to the device, a Power-on Reset is generated. A new Power-on Reset event is generated if the supply voltage falls below the device threshold voltage (VPOR). An internal POR pulse is generated when the rising supply voltage crosses the POR circuit threshold voltage.

6.3 Oscillator Start-up Timer/Stabilizer (OST)

An Oscillator Start-up Timer (OST) is included to ensure that a crystal oscillator (or ceramic resonator) has started and stabilized. The OST is a simple, 10-bit counter that counts 1024 TOSC cycles before releasing the oscillator clock to the rest of the system. The time-out period is designated as TOST. The TOST time is involved every time the oscillator has to restart (i.e., on Power-on Reset (POR) and wake-up from Sleep). The Oscillator Start-up Timer is applied to the LP oscillator, XT and HS modes (upon wake-up from Sleep, POR and BOR) for the primary oscillator.

6.4 Watchdog Timer (WDT)

The primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction. The WDT is a free-running timer that runs off the on-chip LPRC oscillator, requiring no external component. The WDT continues to operate even if the main processor clock (e.g., the crystal oscillator) fails.

The Watchdog Timer can be “Enabled” or “Disabled” either through a configuration bit (FWDTEN) in the Configuration register, or through an SFR bit (SWDTEN).

Any device programmer capable of programming dsPIC® DSC devices (such as Microchip’s MPLAB® PM3 Programmer) allows programming of this and other configuration bits to the desired state. If enabled, the WDT increments until it overflows or “times out”. A WDT time-out forces a device Reset (except during Sleep).

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6.5 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

In the event of an oscillator failure, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. The application program then can either attempt to restart the oscillator, or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

6.6 Reset System

The Reset system combines all Reset sources and controls the device Master Reset signal.

Device Reset sources include:

- POR: Power-on Reset
- BOR: Brown-out Reset
- SWR: `RESET` Instruction
- EXTR: $\overline{\text{MCLR}}$ Reset
- WDTR: Watchdog Timer Time-out Reset
- TRAPR: Trap Conflict
- IOPUWR: Attempted execution of an Illegal Opcode, or Indirect Addressing, using an Uninitialized W register

7.0 DEVICE POWER MANAGEMENT

Power management services provided by the dsPIC33F devices include:

- Real-Time Clock Source Switching
- Power-Saving Modes

7.1 Real-Time Clock Source Switching

Configuration bits determine the clock source upon Power-on Reset (POR) and Brown-out Reset (BOR). Thereafter, the clock source can be changed between permissible clock sources. The OSCCON register controls the clock switching and reflects system clock related status bits. To reduce power consumption, the user can switch to a slower clock source.

7.2 Power-Saving Modes

The dsPIC33F devices have two reduced power modes that can be entered through execution of the `PWRSAV` instruction.

- Sleep Mode: The CPU, system clock source and any peripherals that operate on the system clock source are disabled. This is the lowest power mode of the device.
- Idle Mode: The CPU is disabled but the system clock source continues to operate. Peripherals continue to operate but can optionally be disabled.
- Doze Mode: The CPU clock is temporarily slowed down relative to the peripheral clock by a user-selectable factor.

These modes provide an effective way to reduce power consumption during periods when the CPU is not in use.

7.2.1 SLEEP MODE

When the device enters Sleep mode:

- System clock source is shut down. If an on-chip oscillator is used, it is turned off.
- Device current consumption is at minimum provided that no I/O pin is sourcing current.
- Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode because the system clock source is disabled.
- LPRC clock continues to run in Sleep mode if the WDT is enabled.
- BOR circuit, if enabled, remains operative during Sleep mode
- WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some peripherals may continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, or peripherals that use an external clock input. Any peripheral that is operating on the system clock source is disabled in Sleep mode.

The processor exits (wakes up) from Sleep on one of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

7.2.2 IDLE MODE

When the device enters Idle mode:

- CPU stops executing instructions
- WDT is automatically cleared
- System clock source remains active
- Peripheral modules, by default, continue to operate normally from the system clock source
- Peripherals, optionally, can be shut down in Idle mode using their ‘stop-in-idle’ control bit.
- If the WDT or FSCM is enabled, the LPRC also remains active

The processor wakes from Idle mode on these events:

- Any interrupt that is individually enabled
- Any source of device Reset
- A WDT time-out

Upon wake-up from Idle, the clock is re-applied to the CPU and instruction execution begins immediately starting with the instruction following the `PWRSAV` instruction, or the first instruction in the Interrupt Service Routine (ISR).

7.2.3 DOZE MODE

The Doze mode provides the user software the ability to temporarily reduce the processor instruction cycle frequency relative to the peripheral frequency. Clock frequency ratios of 1:1, 1:2, 1:4, 1:8, 1:16, 1:32, 1:64 and 1:128 are supported.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps bit rate based on this device operating speed. If the device is now placed in Doze mode with a clock frequency ratio of 1:4, the CAN module will continue to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

This feature further reduces the power consumption during periods where relatively less CPU activity is required.

When the device is operating in Doze mode, the hardware ensures that there is no loss of synchronization between peripheral events and SFR accesses by the CPU.

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8.0 dsPIC33F PERIPHERALS

The Digital Signal Controller (DSC) family of 16-bit DSC devices provides the integrated functionality of many peripherals. Specific peripheral functions include:

- Analog-to-Digital Converters
  - 10-bit High-Speed A/D Converter
  - 12-bit High-Resolution A/D Converter
- General Purpose 16-Bit Timers
- Motor Control PWM module
- Quadrature Encoder Interface module
- Input Capture module
- Output Compare/PWM module
- Data Converter Interface
- Serial Peripheral Interface (SPI™) module
- UART module
- I^2C™ module
- Controller Area Network (CAN) module
- I/O pins

8.1 Analog-to-Digital Converters

The Analog-to-Digital (A/D) Converters provide up to 32 analog inputs with both single-ended and differential inputs. These modules offer on-board sample and hold circuitry.

To minimize control loop errors due to finite update times (conversion plus computations), a high-speed low-latency ADC is required.

In addition, several hardware features have been included in the peripheral interface to improve real-time performance in a typical DSP-based application.

- Result alignment options
- Automated sampling
- Automated channel scanning
- Dual port data buffer
- External conversion start control

The A/D Converter is available in either of the following configurations:

- 10-bit, 1.1 Msps A/D module:
  - 2.2 Msps A/D conversion using 2 channels
- 12-bit, 500 ksps A/D module:
  - 1 Msps A/D conversion using 2 channels

Key features of the A/D module include:

- 10-bit or 12-bit resolution
- Unipolar differential sample/hold amplifiers
- Up to 32 input channels
- Selectable voltage reference sources
  - External V_{REF+} and V_{REF-} pins available
- ±1 LSB max Differential Nonlinearity (DNL) (3.3V ±10%)
- ±1 LSB max Integral Nonlinearity (INL) (3.3V ±10%)
- Up to 4 on-chip sample and hold amplifiers in each A/D
  - Enables simultaneous sampling of 2, 4 or 8 analog inputs
- Automated channel scanning
- Single-supply operation: 3.0-3.6V
- 2.2 Msps or 1 Msps sampling rate at 3.0V
- Ability to convert during CPU Sleep and Idle modes
- Conversion start can be manual or synchronized with 1 of 4 trigger sources (automatic, Timer3, external interrupt, PWM period match)
- A/D can use DMA for buffer storage
- Lower and upper half of buffer can be filled on alternate conversions

8.2 General Purpose Timer Modules

The General Purpose (GP) timer modules provide the time base elements for input capture and output compare/PWM. They can be configured for Real-Time Clock operation as well as various timer/counter modes. The timer modes count pulses of the internal time base, whereas counter modes count external pulses that appear on the timer clock pin.

The dsPIC33F device supports up to nine 16-bit timers (Timer1 through Timer9). Eight of the 16-bit timers can be configured as four 32-bit timers (Timer2/3, Timer4/5, Timer6/7 and Timer8/9). Each timer has several selectable operating modes.

8.2.1 TIMER1

The Timer1 module (Figure 8-1) is a 16-bit timer that can serve as the time counter for an asynchronous Real-Time Clock, or operate as a free-running interval timer/counter. The 16-bit timer has the following modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

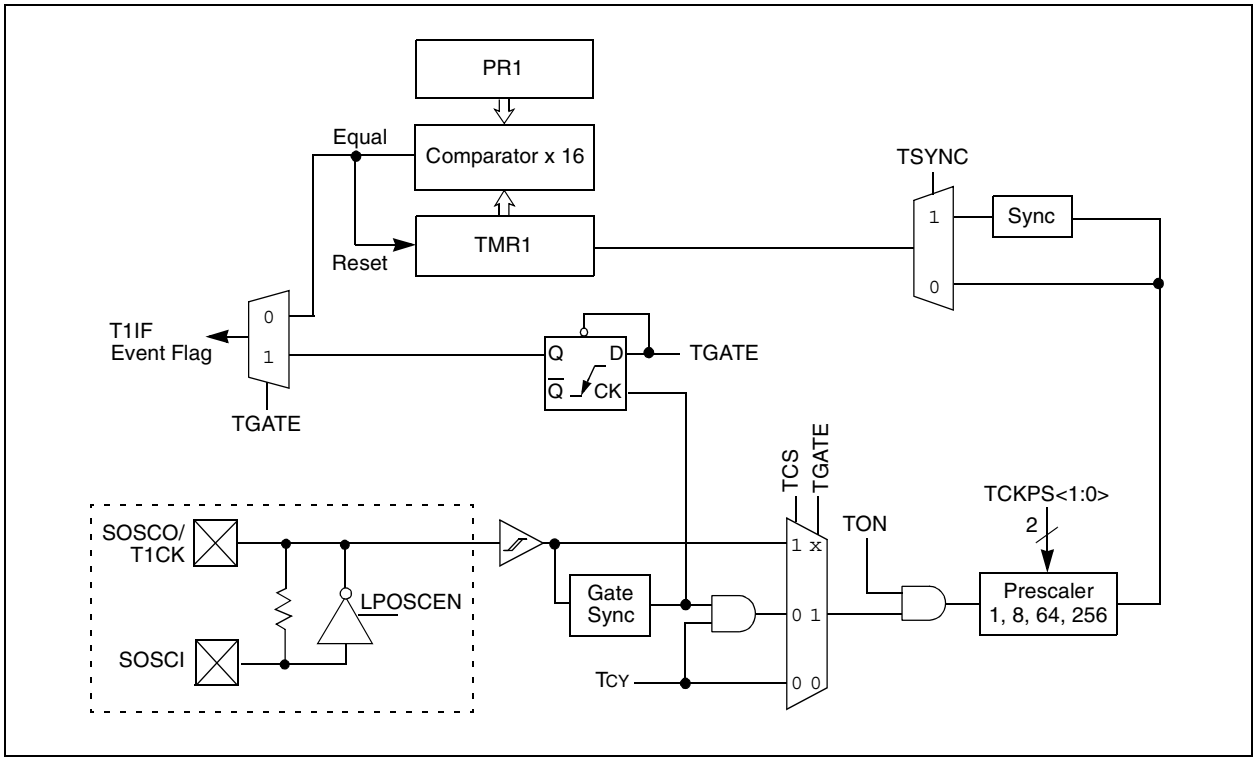
Further, the following operational characteristics are supported:

- Timer gated by external pulse
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-Bit Period register match or falling edge of external gate signal

Timer1, when operating in Real-Time Clock (RTC) mode, provides time of day and event time-stamping capabilities. Key operational features of the RTC are:

- Operation from 32 kHz LP oscillator
- 8-bit prescaler
- Low power
- Real-Time Clock interrupts

FIGURE 8-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



8.2.2 TIMER2/3

The Timer2/3 module is a 32-bit timer (which can be configured as two 16-bit timers) with selectable operating modes. These timers are used by other peripheral modules, such as:

- Input Capture
- Output Compare/Simple PWM

Timer2/3 has the following modes:

- Two independent 16-bit timers (Timer2 and Timer3) with Timer and Synchronous Counter modes
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

Further, the following operational characteristics are supported:

- ADC conversion start trigger
- 32-bit timer gated by external pulse
- Selectable prescaler settings
- Timer counter operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period register match
- Timer2/3 can use DMA for buffer storage

8.2.3 TIMER4/5, TIMER6/7, TIMER8/9

The Timer4/5, Timer6/7 and Timer8/9 modules are similar in operation to the Timer2/3 module. Differences include:

- These modules do not support the ADC event trigger feature
- These modules can not be used by other peripheral modules, such as input capture and output compare

8.3 Motor Control PWM Module

The Motor Control PWM (MCPWM) module simplifies the task of generating multiple, synchronized pulse-width modulated outputs. In particular, the following power and motion control applications are supported:

- Three-Phase AC Induction Motor
- Switched Reluctance (SR) Motor
- Brushless DC (BLDC) Motor
- Uninterrupted Power Supply (UPS)

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The PWM module has the following features:

- Dedicated time base supports TCY/2 PWM edge resolution
- Two output pins (pair) for each PWM generator
- Complementary or independent operation for each output pin pair
- Hardware dead-time generators for Complementary mode
- Output pin polarity defined by nonvolatile device configuration bits
- Multiple output modes:
  - Edge-Aligned mode
  - Center-Aligned mode
  - Center-Aligned mode with double updates
  - Single Event mode
- Manual override register for PWM output pins
- Hardware Fault input pins with programmable function
- Trigger for synchronizing A/D samples and conversions to PWM timing
- Each output pin associated with the PWM can be individually enabled

8.3.1 PWM TIME BASE

The PWM time base is provided by a 15-bit timer with a prescaler and postscaler. The PWM time base can be configured for four different modes of operation:

- Free-Running mode
- Single-Shot mode
- Continuous Up/Down Count mode
- Continuous Up/Down Count mode with interrupts for double updates

The Up/Down Counting modes support center-aligned PWM generation. The Single-Shot mode allows the PWM module to support pulse control of certain Electronically Commutated Motors (ECMs).

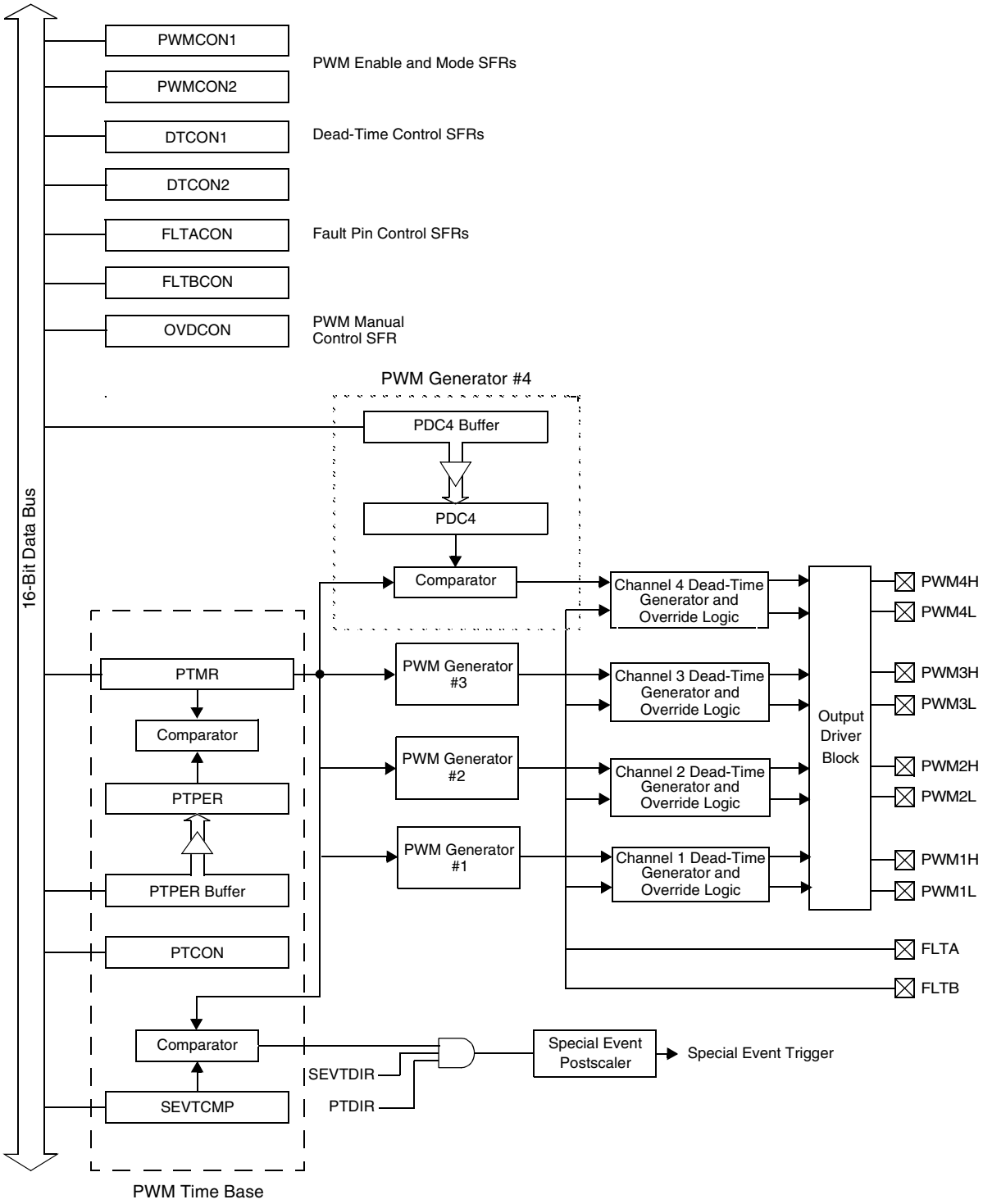
Table 8-1 lists the frequencies and resolutions that can be attained as a function of the dsPIC33F device instruction cycle frequency.

TABLE 8-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS, 1:1 PRESCALER

TCY (FCY)	PTPER Value	PWM Resolution	PWM Frequency*
25 ns (40 MHz)	0x7FFF	16 bits	1220 Hz
25 ns (40 MHz)	0x03FF	11 bits	39.1 kHz
50 ns (20 MHz)	0x7FFF	16 bits	610 Hz
50 ns (20 MHz)	0x01FF	10 bits	39.1 kHz
100 ns (10 MHz)	0x7FFF	16 bits	305 Hz
100 ns (10 MHz)	0x00FF	9 bits	39.1 kHz
200 ns (5 MHz)	0x7FFF	16 bits	153 Hz
200 ns (5 MHz)	0x007F	8 bits	39.1 kHz

***** PWM frequencies will be 1/2 the value indicated for center-aligned operation.

FIGURE 8-2: 8-OUTPUT PWM MODULE BLOCK DIAGRAM



Note: Details of PWM Generator #1, #2 and #3 are not shown for clarity.

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8.4 Quadrature Encoder Interface (QEI) Module

Quadrature encoders (also referred to as incremental encoders or optical encoders) are used in position and speed detection of rotating motion systems. Quadrature encoders enable closed-loop control of many motor control applications, such as Switched Reluctance (SR) Motor and AC Induction Motor (ACIM).

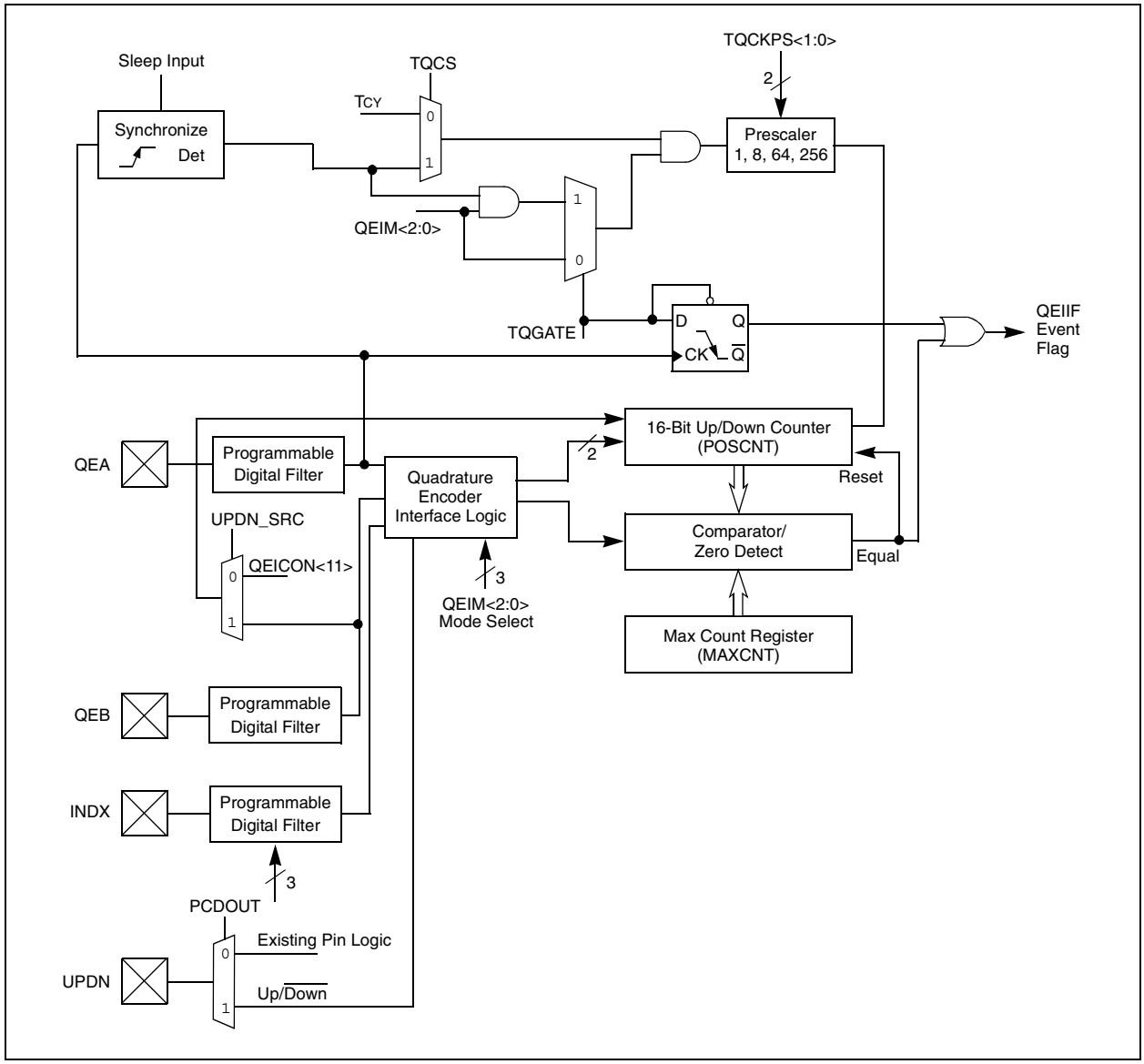
Typically, three outputs termed, Phase A, Phase B and INDEX, provide information that can be decoded to provide information on the movement of the motor shaft, including distance and direction.

A quadrature decoder captures the phase signals and index pulse and converts the information into a numeric count of the position pulses. Generally, the count will increment when the shaft is rotating one direction and decrement when the shaft is rotating in the other direction.

The QEI module (Figure 8-3) includes:

- Three input pins for two phase signals and index pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- 16-bit up/down position counter
- Count direction status
- x2 and x4 count resolution
- Two modes of Position Counter Reset
- General Purpose16-Bit Timer/Counter mode
- Interrupts generated by QEI or counter events

FIGURE 8-3: QUADRATURE ENCODER INTERFACE BLOCK DIAGRAM



8.5 Input Capture Module

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33F devices support up to eight input capture channels.

The input capture module captures the 16-bit value of the selected time base register when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling)
3. Prescaler Capture Event modes
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base. The selected timer can use either an internal or an external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts.

Input capture channels IC1 and IC2 support DMA data transfers.

8.6 Output Compare/PWM Module

The output compare module features are quite useful in applications that require controlled timing pulses or PWM modulated pulse streams.

The output compare module has the ability to compare the value of a selected time base with the value of one or two compare registers (depending on the operation mode selected). Furthermore, it has the ability to generate a single output pulse, or a repetitive sequence of output pulses, on a compare match event. Like most dsPIC33F peripherals, it also has the ability to generate interrupts on compare match events.

The dsPIC33F device may have up to eight output compare channels, designated OC1 through OC8. Refer to the specific device data sheet for the number of channels available in a particular device. All output compare channels are functionally identical.

Each output compare channel can use one of two selectable time bases. The time base is selected using the OCTSEL bit (OCxCON<3>). An ‘x’ in the pin, register or bit name denotes the specific output compare channel. Refer to the device data sheet for the specific timers that can be used with each output compare channel number.

Each output compare module has the following modes of operation:

- Single Compare Match mode
- Dual Compare Match mode generating
  - Single Output Pulse
  - Continuous Output Pulses
- Simple Pulse-Width Modulation mode
  - With Fault Protection Input
  - Without Fault Protection Input

Output compare channels, OC1 and OC2, support DMA data transfers.

8.7 Data Converter Interface Module

The dsPIC33F Data Converter Interface (DCI) module allows simple interfacing to devices such as audio coder/decoders (codecs), A/D Converters and D/A Converters.

The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I^2S) Interface
- AC-Link (AC’97) Compliant mode

Many codecs intended for use in audio applications support sampling rates between 8 kHz and 48 kHz and use one of the interface protocols listed above. The DCI automatically handles the interface timing associated with these codecs. No overhead from the CPU is required until the requested amount of data has been transmitted and/or received by the DCI. Up to four data words can be transferred between CPU interrupts.

The data word length for the DCI is programmable up to 16 bits to match the data size of the dsPIC33F CPU. However, many codecs have data word sizes greater than 16 bits. Long data word lengths can be supported by the DCI. The DCI is configured to transmit/receive the long word in multiple 16-bit time slots. This operation is transparent to the user and the long data word is stored in consecutive register locations.

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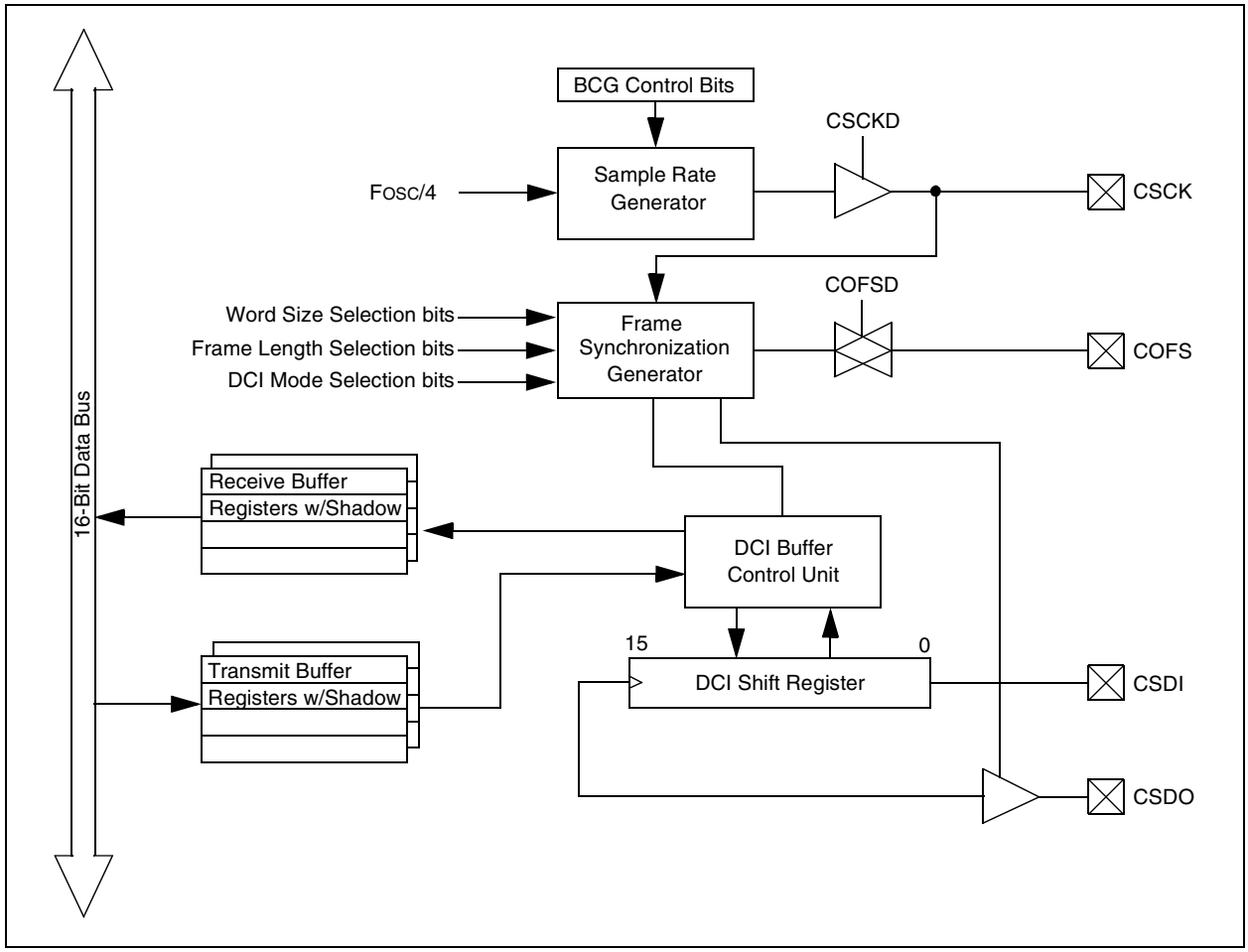
Figure 8-4 is a block diagram of the DCI module. The DCI can support up to 16 time slots in a data frame for a maximum frame size of 256 bits. There are control bits for each time slot in the data frame that determine whether the DCI will transmit/receive during the time slot. The DCI module supports DMA data transfers.

FIGURE 8-4: DCI MODULE BLOCK DIAGRAM



8.8 SPI™ Module

The Serial Peripheral Interface (SPI) module is a synchronous serial interface for communicating with other peripheral or microcontroller devices such as serial EEPROMs, shift registers, display drivers, A/D Converters, etc. It is compatible with Motorola® SPI and SIOP interfaces.

This SPI module includes all SPI modes. A Frame Synchronization mode is also included for support of voice band codecs.

Four pins make up the serial interface: SDI, Serial Data Input; SDO, Serial Data Output; SCK, Shift Clock Input or Output; $\overline{SS}$, Active-Low Slave Select, which also serves as the FSYNC (Frame Synchronization Pulse). A device set up as an SPI master provides the serial communication clock signal on its SCK pin.

A series of 8 or 16 clock pulses (depending on mode) shift out the 8 or 16 bits (depending on whether a byte or word is being transferred) and simultaneously shift in 8 or 16 bits of data from the SDI pin. An interrupt is generated when the transfer is complete.

Slave select synchronization allows selective enabling of SPI slave devices, which is particularly useful when a single master is connected to multiple slaves.

The SPI1 and SPI2 modules support DMA data transfers.

8.9 UART Module

The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, RS-232 and RS-485 interfaces.

The dsPIC33F devices have one or more UARTs.

The key features of the UART module are:

- Full-duplex operation with 8 or 9-bit data
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates range from up to 10 Mbps and down to 38 Hz at 40 MIPS
- 4-character deep transmit data buffer
- 4-character deep receive data buffer
- Parity, framing and buffer overrun error detection
- Full IrDA® support, including hardware encoding and decoding of IrDA® messages
- LIN bus support
  - Auto wake-up from Sleep or Idle mode on Start bit detect
  - Auto-baud detection
  - Break character support
- Support for interrupt on address detect (9th bit = 1)
- Separate transmit and receive interrupts
  - On transmission of 1 or 4 characters
  - On reception of 1, 3 and 4 characters
- Loopback mode for diagnostics

The UART1 and UART2 modules support DMA data transfers.

8.10 I²C™ Module

The I²C module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc.

The Inter-Integrated Circuit (I²C) module offers full hardware support for both slave and multi-master operations.

The key features of the I²C module are:

- I²C slave operation supports 7 and 10-bit address
- I²C master operation supports 7 and 10-bit address
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (serial clock stretching)
- I²C supports multi-master operation; detects bus collision and will arbitrate accordingly
- Slew rate control for 100 kHz and 400 kHz bus speeds

In I²C mode, pin SCL is clock and pin SDA is data. The module will override the data direction bits for these pins.

8.11 Controller Area Network (CAN) Module

The Controller Area Network (CAN) module is a serial interface useful for communicating with other CAN modules or microcontroller devices. This interface/ protocol was designed to allow communications within noisy environments.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH specification. The module supports CAN 1.2, CAN 2.0A, CAN2.0B Passive and CAN 2.0B Active versions of the protocol. Details of these protocols can be found in the BOSCH CAN specification.

The CAN module features:

- Implementation of the CAN protocol CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and extended data frames
- Data lengths of 0-8 bytes
- Programmable bit rate up to 1 Mbit/sec
- Automatic response to remote frames
- Up to 16 receive buffers in DMA RAM
- FIFO Buffer mode (up to 64 messages deep)
- 16 full (standard/extended identifier) acceptance filters
- 3 full acceptance filter masks
- Up to 8 transmit buffers in DMA RAM
- DMA can be used for transmission and reception
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation
- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- Programmable clock source
- Programmable link to timer module for time-stamping and network synchronization
- Low-power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

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8.12 I/O Pins

Some pins for the I/O pin functions are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

All I/O port pins have three registers directly associated with the operation of the port pin. The Data Direction register determines whether the pin is an input or an output. The Port Data Latch register provides latched output data for the I/O pins. The Port register provides visibility of the logic state of the I/O pins. Reading the Port register provides the I/O pin logic state, while writes to the Port register write the data to the Port Data Latch register.

I/O port pins have latch bits (Port Data Latch register). This register, when read, yields the contents of the I/O latch and when written, modifies the contents of the I/O latch, thus modifying the value driven out on a pin if the corresponding Data Direction register bit is configured for output. This can be used in read-modify-write instructions that allow the user to modify the contents of the Port Data Latch register, regardless of the status of the corresponding pins.

The I/O pins have the following features:

- Schmitt Trigger input
- CMOS output drivers
- Weak internal pull-up

All I/O pins configured as digital inputs can accept 5V signals. This provides a degree of compatibility with external signals of different voltage levels. However, all digital outputs and analog pins can only generate voltage levels up to 3.6V.

The input change notification module gives dsPIC33F devices the ability to generate interrupt requests to the processor in response to a change of state on selected input pins. This module is capable of detecting input changes of state, even in Sleep mode, when the clocks are disabled. There are up to 24 external signals (CN0 through CN23) that can be selected (enabled) for generating an interrupt request on a change of state. Each of the CN pins also has an optional weak pull-up feature.

9.0 dsPIC33F INSTRUCTION SET

9.1 Introduction

The dsPIC33F instruction set provides a broad suite of instructions which supports traditional microcontroller applications, and a class of instructions which supports math-intensive applications. Since almost all of the functionality of the PICmicro® MCU instruction set has been maintained, this hybrid instruction set allows a friendly DSP migration path for users already familiar with the PICmicro microcontroller.

9.2 Instruction Set Overview

The dsPIC33F instruction set contains 84 instructions which can be grouped into the ten functional categories shown in Table 9-1. Table 9-2 defines the symbols used in the instruction summary tables, Table 9-3 through Table 9-12. These tables define the syntax, description, storage and execution requirements for each instruction. Storage requirements are represented in 24-bit instruction words and execution requirements are represented in instruction cycles. Most instructions have several different addressing modes and execution flows which require different instruction variants. For instance, there are six unique `ADD` instructions and each instruction variant has its own instruction encoding.

TABLE 9-1: dsPIC33F INSTRUCTION GROUPS

Functional Group	Summary Table
Move Instructions	Table 9-3
Math Instructions	Table 9-4
Logic Instructions	Table 9-5
Rotate/Shift Instructions	Table 9-6
Bit Instructions	Table 9-7
Compare/Skip Instructions	Table 9-8
Program Flow Instructions	Table 9-9
Shadow/Stack Instructions	Table 9-10
Control Instructions	Table 9-11
DSP Instructions	Table 9-12

9.2.1 MULTI-CYCLE INSTRUCTIONS

As the instruction summary tables show, most instructions execute in a single cycle with the following exceptions:

- Instructions `DO, MOV.D, POP.D, PUSH.D, TBLRDH, TBLRDL, TBLWTH` and `TBLWTL` require 2 cycles to execute.
- Instructions `DIVF, DIV.S, DIV.U` are single-cycle instructions, which should be executed 18 consecutive times as the target `REPEAT` instruction.
- Instructions that change the program counter also require 2 cycles to execute, with the extra cycle executed as a `NOP`. Skip instructions, which skip over a 2-word instruction, require 3 instruction cycles to execute with 2 cycles executed as a `NOP`.
- The `RETFIE, RETLW` and `RETURN` are special cases of instructions that change the program counter. These execute in 3 cycles unless an exception is pending, and then they execute in 2 cycles.

Note:	Instructions that access program memory as data, using Program Space Visibility, incur some cycle count overhead.

9.2.2 MULTI-WORD INSTRUCTIONS

As the instruction summary tables show, almost all instructions consume one instruction word (24 bits), with the exception of the `CALL, DO` and `GOTO` instructions, which are flow instructions listed in Table 9-9. These instructions require two words of memory because their opcodes embed large literal operands.

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TABLE 9-2: SYMBOLS USED IN SUMMARY TABLES

Symbol	Description
#	Literal operand designation
Acc	Accumulator A or Accumulator B
AWB	Accumulator Write Back
bit4	4-bit wide bit position (0:15)
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address
lit1	1-bit literal (0:1)
lit4	4-bit literal (0:15)
lit5	5-bit literal (0:31)
lit8	8-bit literal (0:255)
lit10	10-bit literal (0:255 for Byte mode, 0:1023 for Word mode)
lit14	14-bit literal (0:16383)
lit16	16-bit literal (0:65535)
lit23	23-bit literal (0:8388607)
Slit4	Signed 4-bit literal (-8:7)
Slit6	Signed 6-bit literal (-16:16)
Slit10	Signed 10-bit literal (-512:511)
Slit16	Signed 16-bit literal (-32768:32767)
TOS	Top-of-Stack
Wb	Base working register
Wd	Destination working register (direct and indirect addressing)
Wm, Wn	Working register divide pair (dividend, divisor)
Wm*Wm	Working register multiplier pair (same source register)
Wm*Wn	Working register multiplier pair (different source registers)
Wn	Both source and destination working register (direct addressing)
Wnd	Destination working register (direct addressing)
Wns	Source working register (direct addressing)
WREG	Default working register
Ws	Source working register (direct and indirect addressing)
Wx	Source addressing mode and working register for X data bus prefetch
Wxd	Destination working register for X data bus prefetch
Wy	Source addressing mode and working register for Y data bus prefetch
Wyd	Destination working register for Y data bus prefetch

TABLE 9-3: MOVE INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
EXCH	Wns,Wnd	Swap Wns and Wnd	1	1
MOV	f {,WREG}	Move f to destination	1	1
MOV	WREG,f	Move WREG to f	1	1
MOV	f,Wnd	Move f to Wnd	1	1
MOV	Wns,f	Move Wns to f	1	1
MOV.b	#lit8,Wnd	Move 8-bit literal to Wnd	1	1
MOV	#lit16,Wnd	Move 16-bit literal to Wnd	1	1
MOV	[Ws+Slit10],Wnd	Move [Ws + signed 10-bit offset] to Wnd	1	1
MOV	Wns,[Wd+Slit10]	Move Wns to [Wd + signed 10-bit offset]	1	1
MOV	Ws,Wd	Move Ws to Wd	1	1
MOV.D	Ws,Wnd	Move double Ws to Wnd:Wnd + 1	1	2
MOV.D	Wns,Wd	Move double Wns:Wns + 1 to Wd	1	2
SWAP	Wn	Wn = byte or nibble swap Wn	1	1
TBLRDH	Ws,Wd	Read high program word to Wd	1	2
TBLRDL	Ws,Wd	Read low program word to Wd	1	2
TBLWTH	Ws,Wd	Write Ws to high program word	1	2
TBLWTL	Ws,Wd	Write Ws to low program word	1	2

Note: When the optional {,WREG} operand is specified, the destination of the instruction is WREG. When {,WREG} is not specified, the destination of the instruction is the file register f.

Note: Table 9-3 through Table 9-12 present the base instruction syntax for the dsPIC33F. These instructions do not include all of the available addressing modes. For example, some instructions show the Byte Addressing mode and others do not.

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TABLE 9-4: MATH INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
ADD	f {,WREG}	Destination = f + WREG	1	1
ADD	#lit10,Wn	Wn = lit10 + Wn	1	1
ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1
ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1
ADDC	f {,WREG}	Destination = f + WREG + (C)	1	1
ADDC	#lit10,Wn	Wn = lit10 + Wn + (C)	1	1
ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1
ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1
DAW.B	Wn	Wn = decimal adjust Wn	1	1
DEC	f {,WREG}	Destination = f – 1	1	1
DEC	Ws,Wd	Wd = Ws – 1	1	1
DEC2	f {,WREG}	Destination = f – 2	1	1
DEC2	Ws,Wd	Wd = Ws – 2	1	1
DIV.S	Wm,Wn	Signed 16/16-bit integer divide*	1	18
DIV.SD	Wm,Wn	Signed 32/16-bit integer divide*	1	18
DIV.U	Wm,Wn	Unsigned 16/16-bit integer divide*	1	18
DIV.UD	Wm,Wn	Unsigned 32/16-bit integer divide*	1	18
DIVF	Wm,Wn	Signed 16/16-bit fractional divide*	1	18
INC	f {,WREG}	Destination = f + 1	1	1
INC	Ws,Wd	Wd = Ws + 1	1	1
INC2	f {,WREG}	Destination = f + 2	1	1
INC2	Ws,Wd	Wd = Ws + 2	1	1
MUL	f	W3:W2 = f * WREG	1	1
MUL.SS	Wb,Ws,Wnd	{Wnd + 1,Wnd} = sign(Wb) * sign(Ws)	1	1
MUL.SU	Wb,#lit5,Wnd	{Wnd + 1,Wnd} = sign(Wb) * unsign(lit5)	1	1
MUL.SU	Wb,Ws,Wnd	{Wnd + 1,Wnd} = sign(Wb) * unsign(Ws)	1	1
MUL.US	Wb,Ws,Wnd	{Wnd + 1,Wnd} = unsign(Wb) * sign(Ws)	1	1
MUL.UU	Wb,#lit5,Wnd	{Wnd + 1,Wnd} = unsign(Wb) * unsign(lit5)	1	1
MUL.UU	Wb,Ws,Wnd	{Wnd + 1,Wnd} = unsign(Wb) * unsign(Ws)	1	1
SE	Ws,Wnd	Wnd = sign-extended Ws	1	1
SUB	f {,WREG}	Destination = f – WREG	1	1
SUB	#lit10, Wn	Wn = Wn – lit10	1	1
SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1
SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1
SUBB	f {,WREG}	Destination = f – WREG – (C)	1	1
SUBB	#lit10, Wn	Wn = Wn – lit10 – (C)	1	1
SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1
SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1
SUBBR	f {,WREG}	Destination = WREG – f – ($\overline{C}$)	1	1
SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1
SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1
SUBR	f {,WREG}	Destination = WREG – f	1	1
SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1
SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1
ZE	Ws,Wnd	Wnd = zero-extended Ws	1	1

* Divide instructions are interruptible on a cycle-by-cycle basis. Also, divide instructions must be accompanied by a REPEAT instruction, which adds 1 extra cycle.

TABLE 9-5: LOGIC INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
AND	f {,WREG}	Destination = f .AND. WREG	1	1
AND	#lit10,Wn	Wn = lit10 .AND. Wn	1	1
AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1
AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1
CLR	f	f = 0x0000	1	1
CLR	WREG	WREG = 0x0000	1	1
CLR	Wd	Wd = 0x0000	1	1
COM	f {,WREG}	Destination = $\overline{f}$	1	1
COM	Ws,Wd	Wd = $\overline{Ws}$	1	1
IOR	f {,WREG}	Destination = f .IOR. WREG	1	1
IOR	#lit10,Wn	Wn = lit10 .IOR. Wn	1	1
IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1
IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1
NEG	f {,WREG}	Destination = $\overline{f}$ + 1	1	1
NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1
SETM	f	f = 0xFFFF	1	1
SETM	WREG	WREG = 0xFFFF	1	1
SETM	Wd	Wd = 0xFFFF	1	1
XOR	f {,WREG}	Destination = f .XOR. WREG	1	1
XOR	#lit10,Wn	Wn = lit10 .XOR. Wn	1	1
XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1
XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1

Note: When the optional {,WREG} operand is specified, the destination of the instruction is WREG. When {,WREG} is not specified, the destination of the instruction is the file register f.

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TABLE 9-6: ROTATE/SHIFT INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
ASR	f {,WREG}	Destination = arithmetic right shift f	1	1
ASR	Ws,Wd	Wd = arithmetic right shift Ws	1	1
ASR	Wb,#lit4,Wnd	Wnd = arithmetic right shift Wb by lit4	1	1
ASR	Wb,Wns,Wnd	Wnd = arithmetic right shift Wb by Wns	1	1
LSR	f {,WREG}	Destination = logical right shift f	1	1
LSR	Ws,Wd	Wd = logical right shift Ws	1	1
LSR	Wb,#lit4,Wnd	Wnd = logical right shift Wb by lit4	1	1
LSR	Wb,Wns,Wnd	Wnd = logical right shift Wb by Wns	1	1
RLC	f {,WREG}	Destination = rotate left through Carry f	1	1
RLC	Ws,Wd	Wd = rotate left through Carry Ws	1	1
RLNC	f {,WREG}	Destination = rotate left (no Carry) f	1	1
RLNC	Ws,Wd	Wd = rotate left (no Carry) Ws	1	1
RRC	f {,WREG}	Destination = rotate right through Carry f	1	1
RRC	Ws,Wd	Wd = rotate right through Carry Ws	1	1
RRNC	f {,WREG}	Destination = rotate right (no Carry) f	1	1
RRNC	Ws,Wd	Wd = rotate right (no Carry) Ws	1	1
SL	f {,WREG}	Destination = left shift f	1	1
SL	Ws,Wd	Wd = left shift Ws	1	1
SL	Wb,#lit4,Wnd	Wnd = left shift Wb by lit4	1	1
SL	Wb,Wns,Wnd	Wnd = left shift Wb by Wns	1	1

Note: When the optional {,WREG} operand is specified, the destination of the instruction is WREG. When {,WREG} is not specified, the destination of the instruction is the file register f.

TABLE 9-7: BIT INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
BCLR	f,#bit4	Bit clear f	1	1
BCLR	Ws,#bit4	Bit clear Ws	1	1
BSET	f,#bit4	Bit set f	1	1
BSET	Ws,#bit4	Bit set Ws	1	1
BSW.C	Ws,Wb	Write C bit to Ws<Wb>	1	1
BSW.Z	Ws,Wb	Write $\overline{SZ}$ bit to Ws<Wb>	1	1
BTG	f,#bit4	Bit toggle f	1	1
BTG	Ws,#bit4	Bit toggle Ws	1	1
BTST	f,#bit4	Bit test f	1	1
BTST.C	Ws,#bit4	Bit test Ws to C	1	1
BTST.Z	Ws,#bit4	Bit test Ws to SZ	1	1
BTST.C	Ws,Wb	Bit test Ws<Wb> to C	1	1
BTST.Z	Ws,Wb	Bit test Ws<Wb> to SZ	1	1
BTSTS	f,#bit4	Bit test f then set f	1	1
BTSTS.C	Ws,#bit4	Bit test Ws to C then set Ws	1	1
BTSTS.Z	Ws,#bit4	Bit test Ws to SZ then set Ws	1	1
FBCL	Ws,Wnd	Find bit change from left (MSb) side	1	1
FF1L	Ws,Wnd	Find first one from left (MSb) side	1	1
FF1R	Ws,Wnd	Find first one from right (LSb) side	1	1

Note: Bit positions are specified by bit4 (0:15) for word operations.

TABLE 9-8: COMPARE/SKIP INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
BTSC	f,#bit4	Bit test f, skip if clear	1	1 (2 or 3)
BTSC	Ws,#bit4	Bit test Ws, skip if clear	1	1 (2 or 3)
BTSS	f,#bit4	Bit test f, skip if set	1	1 (2 or 3)
BTSS	Ws,#bit4	Bit test Ws, skip if set	1	1 (2 or 3)
CP	f	Compare (f – WREG)	1	1
CP	Wb,#lit5	Compare (Wb – lit5)	1	1
CP	Wb,Ws	Compare (Wb – Ws)	1	1
CP0	f	Compare (f – 0x0000)	1	1
CP0	Ws	Compare (Ws – 0x0000)	1	1
CPB	f	Compare with Borrow (f – WREG – $\overline{C}$)	1	1
CPB	Wb,#lit5	Compare with Borrow (Wb – lit5 – $\overline{C}$)	1	1
CPB	Wb,Ws	Compare with Borrow (Wb – Ws – $\overline{C}$)	1	1
CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if Equal (Wb = Wn)	1	1 (2 or 3)
CPSGT	Wb,Wn	Signed Compare Wb with Wn, Skip if Greater Than (Wb > Wn)	1	1 (2 or 3)
CPSLT	Wb,Wn	Signed Compare Wb with Wn, Skip if Less Than (Wb < Wn)	1	1 (2 or 3)
CPSNE	Wb,Wn	Signed Compare Wb with Wn, Skip if Not Equal (Wb ≠ Wn)	1	1 (2 or 3)

Note 1: Bit positions are specified by bit4 (0:15) for word operations.

2: Conditional skip instructions execute in 1 cycle if the skip is not taken, 2 cycles if the skip is taken over a one-word instruction and 3 cycles if the skip is taken over a two-word instruction.

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TABLE 9-9: PROGRAM FLOW INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
BRA	Expr	Branch unconditionally	1	2
BRA	Wn	Computed branch	1	2
BRA	C,Expr	Branch if Carry (no Borrow)	1	1 (2)
BRA	GE,Expr	Branch if greater than or equal	1	1 (2)
BRA	GEU,Expr	Branch if unsigned greater than or equal	1	1 (2)
BRA	GT,Expr	Branch if greater than	1	1 (2)
BRA	GTU,Expr	Branch if unsigned greater than	1	1 (2)
BRA	LE,Expr	Branch if less than or equal	1	1 (2)
BRA	LEU,Expr	Branch if unsigned less than or equal	1	1 (2)
BRA	LT,Expr	Branch if less than	1	1 (2)
BRA	LTU,Expr	Branch if unsigned less than	1	1 (2)
BRA	N,Expr	Branch if Negative	1	1 (2)
BRA	NC,Expr	Branch if not Carry (Borrow)	1	1 (2)
BRA	NN,Expr	Branch if not Negative	1	1 (2)
BRA	NOV,Expr	Branch if not Overflow	1	1 (2)
BRA	NZ,Expr	Branch if not Zero	1	1 (2)
BRA	OA,Expr	Branch if Accumulator A Overflow	1	1 (2)
BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (2)
BRA	OV,Expr	Branch if Overflow	1	1 (2)
BRA	SA,Expr	Branch if Accumulator A Saturate	1	1 (2)
BRA	SB,Expr	Branch if Accumulator B Saturate	1	1 (2)
BRA	Z,Expr	Branch if Zero	1	1 (2)
CALL	Expr	Call subroutine	2	2
CALL	Wn	Call indirect subroutine	1	2
DO	#lit14,Expr	Do code through PC + Expr, (lit14 + 1) times	2	2
DO	Wn,Expr	Do code through PC + Expr, (Wn + 1) times	2	2
GOTO	Expr	Go to address	2	2
GOTO	Wn	Go to address indirectly	1	2
RCALL	Expr	Relative call	1	2
RCALL	Wn	Computed call	1	2
REPEAT	#lit14	Repeat next instruction (lit14 + 1) times	1	1
REPEAT	Wn	Repeat next instruction (Wn + 1) times	1	1
RETFIE		Return from interrupt enable	1	3 (2)
RETLW	#lit10,Wn	Return with lit10 in Wn	1	3 (2)
RETURN		Return from subroutine	1	3 (2)

Note 1: Conditional branch instructions execute in 1 cycle if the branch is not taken, or 2 cycles if the branch is taken.

2: RETURN normally executes in 3 cycles; however, it executes in 2 cycles if an interrupt is pending.

TABLE 9-10: SHADOW/STACK INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
LNK	#lit14	Link Frame Pointer	1	1
POP	f	Pop TOS to f	1	1
POP	Wd	Pop TOS to Wd	1	1
POP.D	Wnd	Double pop from TOS to Wnd:Wnd + 1	1	2
POP.S		Pop shadow registers	1	1
PUSH	f	Push f to TOS	1	1
PUSH	Ws	Push Ws to TOS	1	1
PUSH.D	Wns	Push double Wns:Wns + 1 to TOS	1	2
PUSH.S		Push shadow registers	1	1
ULNK		Unlink Frame Pointer	1	1

TABLE 9-11: CONTROL INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
CLRWDT		Clear Watchdog Timer	1	1
DISI	#lit14	Disable interrupts for (lit14 + 1) instruction cycles	1	1
NOP		No operation	1	1
NOPR		No operation	1	1
PWRSAV	#lit1	Enter Power-Saving mode lit1	1	1
RESET		Software device Reset	1	1

TABLE 9-12: DSP INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
ADD	Acc	Add accumulators	1	1
ADD	Ws,#Slit4,Acc	16-bit signed add to Acc	1	1
CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Acc	1	1
ED	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean distance (no accumulate)	1	1
EDAC	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean distance	1	1
LAC	Ws,#Slit4,Acc	Load Acc	1	1
MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and accumulate	1	1
MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square and accumulate	1	1
MOVSAC	Acc,Wx,Wxd,Wy,Wyd,AWB	Move Wx to Wxd and Wy to Wyd	1	1
MPY	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wn by Wm to Acc	1	1
MPY	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square to Acc	1	1
MPY.N	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wn by Wm) to Acc	1	1
MSC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and subtract from Acc	1	1
NEG	Acc	Negate Acc	1	1
SAC	Acc,#Slit4,Wd	Store Acc	1	1
SAC.R	Acc,#Slit4,Wd	Store rounded Acc	1	1
SFTAC	Acc,#Slit6	Arithmetic shift Acc by Slit6	1	1
SFTAC	Acc,Wn	Arithmetic shift Acc by (Wn)	1	1
SUB	Acc	Subtract accumulators	1	1

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10.0 MICROCHIP DEVELOPMENT TOOL SUPPORT

Microchip offers comprehensive development tools and libraries to support the dsPIC33F architecture. In addition, the company is partnering with many third party tools manufacturers for additional dsPIC33F device support. Table 10-1 lists development tools that support the dsPIC33F family. The paragraphs that follow describe each of the tools in more detail.

TABLE 10-1: dsPIC33F DEVELOPMENT TOOLS

	Development Tool	Description	Part #	From
Essential Software Tools	**MPLAB® IDE** (see **Section 10.1 MPLAB Integrated Development Environment Software**)	Integrated Development Environment	SW007002	Microchip
	MPLAB ASM30 (see **Section 10.2 MPLAB ASM30 Assembler/Linker/Librarian**)	Assembler (included in MPLAB IDE)	SW007002	Microchip
	MPLAB SIM (see **Section 10.3 MPLAB SIM Software Simulator**)	Software Simulator (Included in MPLAB IDE)	SW007002	Microchip
	MPLAB VDI (see **Section 10.4 MPLAB Visual Device Initializer**)	Visual Device Initializer for dsPIC33F (included in MPLAB IDE)	SW007002	Microchip
	MPLAB C30 (see **Section 10.5 MPLAB C30 C Compiler/Linker/Librarian**)	ANSI C Compiler, Assembler, Linker and Librarian	SW006012	Microchip
Essential Hardware Tools	**MPLAB ICD 2** (see **Section 10.6 MPLAB ICD 2 In-Circuit Debugger**)	In-Circuit Debugger and Device Programmer	DV164005	Microchip
	MPLAB PM3 (see **Section 10.7 MPLAB PM3 Universal Device Programmer**)	Full-Featured Device Programmer, Base Unit	DV007004	Microchip
		Socket Module for 100L TQFP Devices (14 mm x 14 mm)	TBD	Microchip
		Socket Module for 80L TQFP Devices (12 mm x 12 mm)	TBD	Microchip
		Socket Module for 64L TQFP Devices (10 mm x 10 mm)	TBD	Microchip

Legend: TBD = To Be Determined

10.1 MPLAB Integrated Development Environment Software

The MPLAB Integrated Development Environment (IDE) is available at no cost. The MPLAB IDE lets the user edit, compile and emulate from a single user interface, as depicted in Figure 10-1. Code can be designed and developed for the dsPIC® DSC devices in the same design environment as the PICmicro microcontrollers. The MPLAB IDE is a 32-bit Windows® operating system-based application that provides many advanced features for the demanding engineer in a modern, easy-to-use interface. MPLAB IDE integrates:

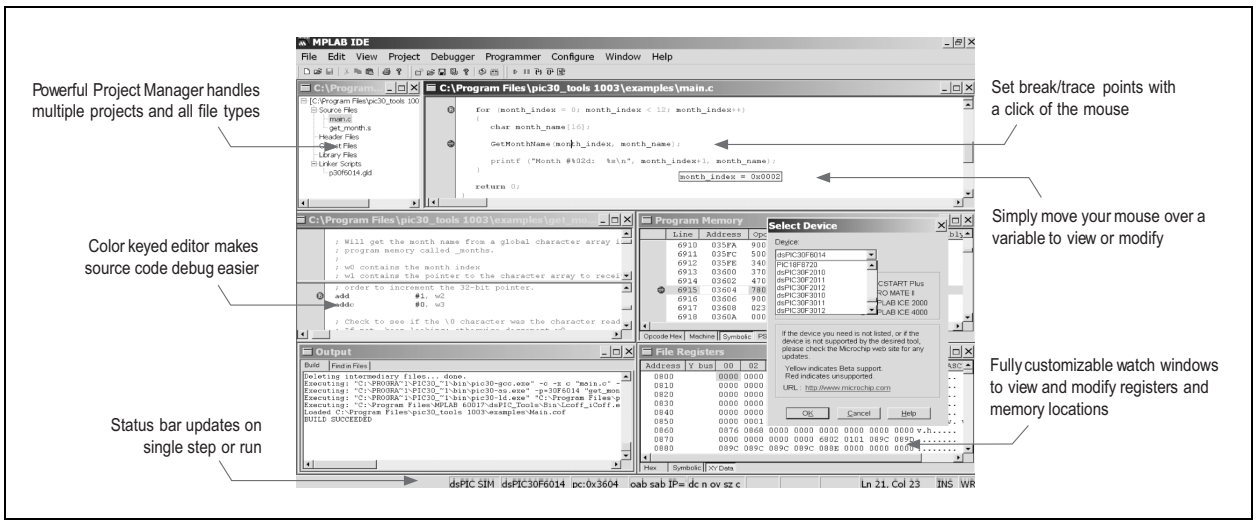
- Full-featured, color coded text editor
- Easy to use project manager with visual display
- Source level debugging
- Enhanced source level debugging for 'C' (structures, automatic variables, etc.)
- Customizable toolbar and key mapping
- Dynamic status bar displays processor condition
- Context sensitive, interactive on-line help
- Integrated MPLAB SIM instruction simulator
- User interface for MPLAB PM3 and PICSTART® Plus device programmers (sold separately)
- User interface for MPLAB ICD 2 In-Circuit Debugger (sold separately)

The MPLAB IDE allows:

- Editing of source files in either assembly or 'C'
- One-touch compiling and downloading to dsPIC DSC emulator or simulator
- Debugging using:
  - Source files
  - Machine code
  - Mixed mode source and machine code

The ability to use the MPLAB IDE with multiple development and debugging targets provides easy transition from the cost-effective simulator to MPLAB ICD 2, or to a full-featured emulator with minimal retraining.

FIGURE 10-1: MPLAB® IDE DESKTOP



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10.2 MPLAB ASM30 Assembler/Linker/ Librarian

MPLAB ASM30 is a full-featured macro assembler. User-defined macros, conditional assembly and a variety of assembler directives make the MPLAB ASM30 a powerful code generation tool.

The accompanying MPLAB LINK30 Linker and MPLAB LIB30 Librarian modules allow efficient linking, library creation and maintenance.

Notable features of the assembler include:

- Support for the entire dsPIC DSC instruction set
- Support for fixed-point and floating-point data
- Available for Windows operating system
- Command Line Interface
- Rich Directive Set
- Flexible Macro Language
- MPLAB IDE compatibility

Notable features of the linker include:

- Automatic or user-defined stack allocation
- Supports dsPIC DSC Program Space Visibility (PSV) window
- Available for Windows operating systems
- Command Line Interface
- Linker scripts for all dsPIC DSC devices
- MPLAB IDE compatibility

10.3 MPLAB SIM Software Simulator

The MPLAB SIM software simulator provides code development for the dsPIC33F family in a PC-hosted environment by simulating the dsPIC33F device on an instruction level. On any instruction, you can examine or modify the data areas and apply stimuli to any of the pins from a file or by pressing a user-defined key.

The execution can be performed in Single-Step, Execute-Until-Break or Trace mode. The MPLAB SIM software simulator fully supports symbolic debugging using the MPLAB C30 C compiler and assembler. The software simulator gives you the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool. Complex stimuli can be injected from files, synchronous clocks or user-defined keys. Output files log register activity for sophisticated post analysis.

Besides modeling the behavior of the CPU, MPLAB SIM also supports the following peripherals:

- Timers
- Input Capture
- 12-Bit ADC
- 10-Bit ADC
- Motor Control PWM
- UART
- I/O Ports
- Program Flash

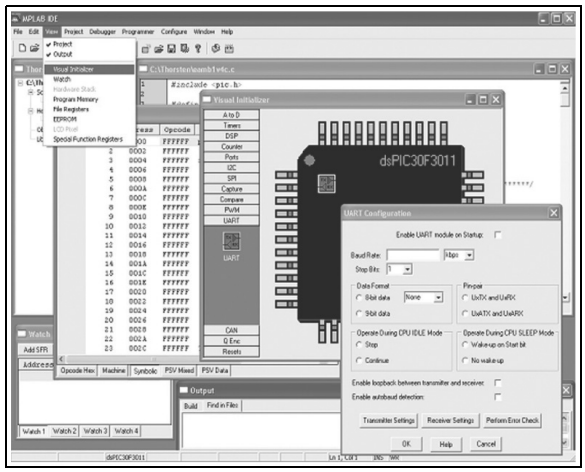
10.4 MPLAB Visual Device Initializer

The MPLAB Visual Device Initializer (VDI) simplifies the task of configuring the dsPIC33F. MPLAB VDI software allows you to configure the entire processor graphically (see Figure 10-2). And when you're done, a mouse click generates your code in assembly or 'C' code. MPLAB VDI performs extensive error checking on assignments and conflicts on pins, memories and interrupts, as well as selection of operating conditions. Generated code files are integrated seamlessly with the rest of our application code through MPLAB Project.

Detailed resource assignment and configuration reports simplify project documentation. Key features of MPLAB VDI include:

- Drag-and-drop feature selection
- One click configuration
- Extensive error checking
- Generates initialization code in the form of a 'C' callable assembly function
- Integrates seamlessly in MPLAB Project
- Printed reports ease project documentation requirements
- MPLAB Visual Device Initializer is an MPLAB plug-in and can be installed independently of MPLAB IDE

FIGURE 10-2: MPLAB® VDI DISPLAY



10.5 MPLAB C30 C Compiler/Linker/ Librarian

The Microchip Technology MPLAB C30 C Compiler provides 'C' language support for the dsPIC33F family. This C compiler is a fully ANSI-compliant product with standard libraries. It is highly optimized for the dsPIC33F family and takes advantage of many dsPIC33F architecture-specific features to help you generate very efficient software code. Figure 10-3 illustrates the code size efficiency relative to several competitors.

MPLAB C30 also provides extensions that allow for excellent support of the hardware, such as interrupts and peripherals. It is fully integrated with MPLAB IDE for high-level source debugging.

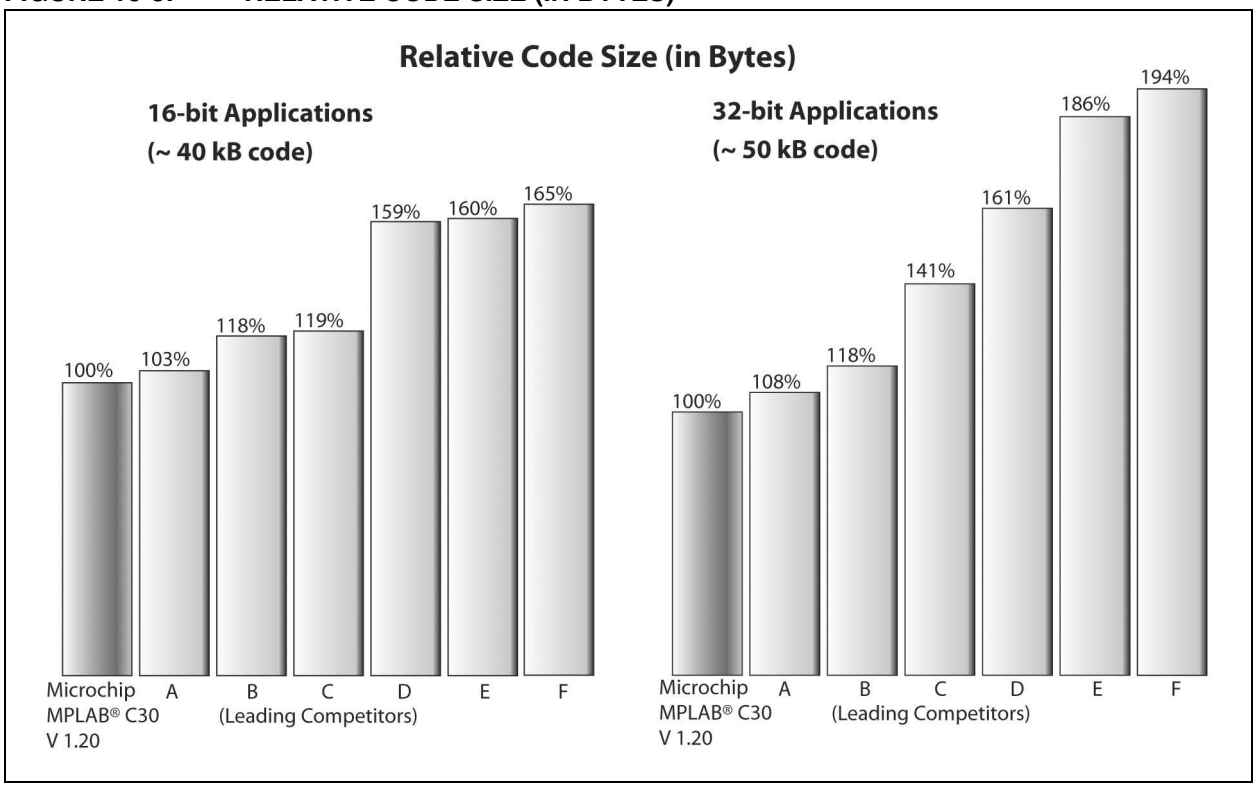
The MPLAB C30 has these characteristics:

- 16-bit native data types
- Efficient use of register-based, 3-operand instructions
- Complex addressing modes
- Efficient multi-bit shift operations
- Efficient signed/unsigned comparisons

MPLAB C30 comes complete with its own assembler, linker and librarian. These allow Mixed mode 'C' and assembly programs and link the resulting object files into a single executable file. The compiler is sold separately. The assembler, linker and librarian are available for free with MPLAB C30.

MPLAB C30 also includes the Math Library, Peripheral Library, DSP Library and standard 'C' libraries.

FIGURE 10-3: RELATIVE CODE SIZE (IN BYTES)



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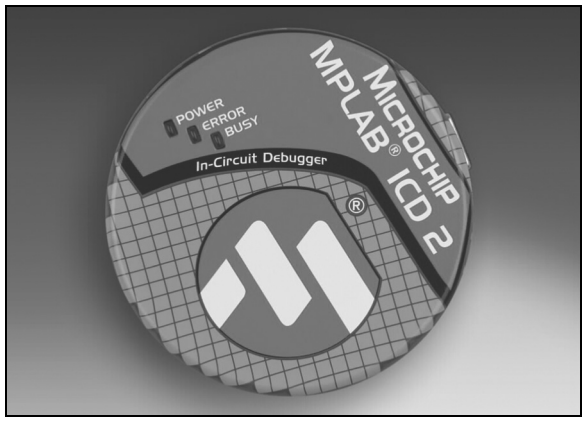
10.6 MPLAB ICD 2 In-Circuit Debugger

The MPLAB ICD 2 In-Circuit Debugger is a powerful, low-cost, run-time development tool that uses in-circuit debugging capability built into the dsPIC33F Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, gives you cost-effective, in-circuit debugging from the graphical user interface of MPLAB IDE. It lets you develop and debug source code by watching variables, single-stepping and setting breakpoints, as well as running at full speed to test hardware in real time.

The MPLAB ICD 2 has these features:

- Full-speed operation to the range of the device
- Serial or USB PC connector
- USB-powered from PC interface
- Low noise power (V_{PP} and V_{DD}) for use with analog and other noise sensitive applications
- Operation down to 2.0V
- Can be used as debugger and inexpensive serial programmer
- Some device resources required (80 bytes of RAM and 2 pins)

FIGURE 10-4: MPLAB® ICD 2 IN-CIRCUIT DEBUGGER



10.7 MPLAB PM3 Universal Device Programmer

The MPLAB PM3 Universal Device Programmer is easy to use with a PC, or as a stand-alone unit, to program Microchip's entire line of PICmicro devices as well as the latest dsPIC33F DSC devices. The MPLAB PM3 features a large and bright LCD unit (128 x 64 pixels) to display easy menus, programming statistics and status information.

The MPLAB PM3 programmer has exceptional programming speed for high production throughput, especially important for large memory devices. It also includes a Secure Digital/Multimedia Card slot for easy and secure data storage and transfer.

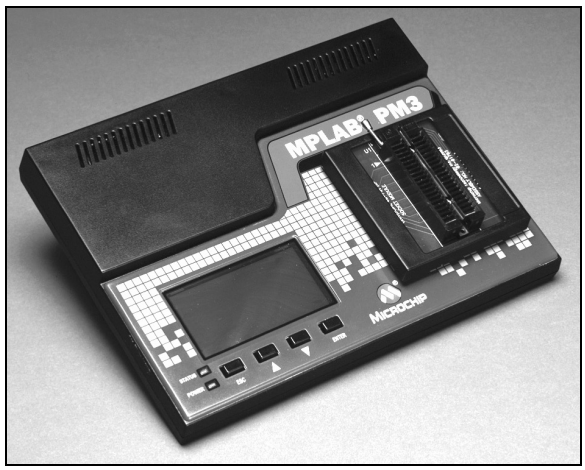
The MPLAB PM3 programmer is designed with 40 programmable socket pins and therefore, each socket module can be configured to support many different devices. As a result, fewer socket modules are required to support the entire line of Microchip parts. The socket modules use multi-pin connectors for high reliability and quick interchange.

When connected to a PC host system, the MPLAB PM3 programmer is seamlessly integrated with the MPLAB Integrated Development Environment (IDE), providing a user-friendly programming interface.

Key features of the MPLAB PM3 Programmer include:

- RS-232 or USB interface
- Integrated In-Circuit Serial Programming™ (ICSP™) interface
- Fast programming time
- Three operating modes:
  - PC Host mode for full control
  - Safe mode for secure data
  - Stand-Alone mode for programming without a PC
- Complete line of interchangeable socket modules to support all Microchip devices and package options (sold separately)
- SQTP^{SM} serialization for programming unique serial numbers while in PC Host mode.
- An alternate DOS command line interface for batch control
- Large easy-to-read display
- Field upgradeable firmware allows quick new device support
- Secure Digital (SD) and Multimedia Card (MMC) external memory support
- Buzzer notification for noisy environments

FIGURE 10-5: MPLAB® PM3 DEVICE PROGRAMMER



11.0 dsPIC33F DEVELOPMENT TOOLS AND APPLICATION LIBRARIES

Microchip offers a comprehensive set of tools and libraries to help with rapid development of dsPIC33F device-based application(s).

Table 11-1 summarizes available and planned dsPIC33F software tools and libraries. Microchip also provides value added services, such as skilled/certified technical application contacts, reference designs and hardware and software developers. (Contact Microchip DSCD Marketing for availability.)

TABLE 11-1: MICROCHIP SOFTWARE DEVELOPMENT TOOLS AND APPLICATION LIBRARIES

Development Tool	Description	Part #
Math Library (see **Section 11.1 Math Library**)	Double Precision and Floating-Point Library (ASM, C Wrapper)	SW300020
Peripheral Library (see **Section 11.2 Peripheral Driver Library**)	Peripheral Initialization, Control and Utility Routines (C)	SW300021
DSP Library (see **Section 11.3 DSP Algorithm Library**)	Essential DSP Algorithm Suite (Filters, FFT)	SW300022
dsPICworks™ Tool (see **Section 11.4 dsPICworks™ Data Analysis and DSP Software**)	Graphical Data Analysis and Conversion Tool for DSP Algorithms	SW300023
Digital Filter Design (see **Section 11.5 Digital Filter Design Software Utility**)	Graphical IIR and FIR Filter Design Package for dsPIC33F	SW300001
TCP/IP Library (see **Section 11.6 Microchip TCP/IP Stack**)	TCP/IP Connectivity and Protocol Support	SW300024
Soft Modem Library (see **Section 11.7 Soft Modem Library**)	V.22bis/V.22 Soft Modem Library	SW300002
	V.32bis Soft Modem Library up to 5K units	SW300003-5K
	V.32bis Soft Modem Library up to 25K units	SW300003-25K
	V.32bis Soft Modem Library up to 100K units	SW300003-100K
	Evaluation Copy of V.32bis Soft Modem Library	SW300003-EVAL
Speech Recognition Library (see **Section 11.8 Speech Recognition Library**)	Speech Recognition Library up to 5K units	SW300010-5K
	Speech Recognition Library up to 25K units	SW300010-25K
	Speech Recognition Library up to 100K units	SW300010-100K
	Evaluation Copy of Speech Recognition Library	SW300010-EVAL
Noise Suppression Library (see **Section 11.9 Noise Suppression Library**)	Noise Suppression Library up to 5K units	SW300040-5K
	Noise Suppression Library up to 25K units	SW300040-25K
	Noise Suppression Library up to 100K units	SW300040-100K
	Evaluation Copy of Noise Suppression Library	SW300040-EVAL
Acoustic Echo Cancellation Library (see **Section 11.10 Acoustic Echo Cancellation Library**)	Acoustic Echo Cancellation Library up to 5K units	SW300060-5K
	Acoustic Echo Cancellation Library up to 25K units	SW300060-25K
	Acoustic Echo Cancellation Library up to 100K units	SW300060-100K
	Evaluation Copy of Acoustic Echo Cancellation Library	SW300060-EVAL
Symmetric Key Embedded Encryption Library (see **Section 11.11 Symmetric Key Embedded Encryption Library**)	Symmetric Key Embedded Encryption Library up to 5K units	SW300050-5K
	Symmetric Key Embedded Encryption Library up to 25K units	SW300050-25K
	Symmetric Key Embedded Encryption Library up to 100K units	SW300050-100K
	Evaluation Copy of Symmetric Key Embedded Encryption Library	SW300050-EVAL
Asymmetric Key Embedded Encryption Library (see **Section 11.12 Asymmetric Key Embedded Encryption Library**)	Asymmetric Key Embedded Encryption Library up to 5K units	SW300055-5K
	Asymmetric Key Embedded Encryption Library up to 25K units	SW300055-25K
	Asymmetric Key Embedded Encryption Library up to 100K units	SW300055-100K
	Evaluation Copy of Asymmetric Key Embedded Encryption Library	SW300055-EVAL
Speech Encoding/Decoding Library (see **Section 11.13 Speech Encoding/Decoding Library**)	Speech Encoding/Decoding Library up to 5K units	SW300070-5K
	Speech Encoding/Decoding Library up to 25K units	SW300070-25K
	Speech Encoding/Decoding Library up to 100K units	SW300070-100K
	Evaluation Copy of Speech Encoding/Decoding Library	SW300070-EVAL

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11.1 Math Library

The dsPIC33F Math Library is the compiled version of the math library that is distributed with the highly optimized, ANSI-compliant dsPIC33F MPLAB C30 C Compiler (SW006012). It contains advanced single and double-precision floating-point arithmetic and trigonometric functions from the standard 'C' header file (`math.h`). The library delivers small program code size and data size, reduced cycles and high accuracy.

Features

- The math library is callable from either MPLAB C30 or dsPIC33F assembly language.
- The functions are IEEE-754 compliant, with signed zero, signed infinity, NaN (Not a Number) and denormal support and operated in the "Round to Nearest" mode.
- Compatible with MPLAB ASM30 and MPLAB LINK30, which are available at no charge from Microchip's web site.

Table 11-2 shows the memory usage and performance of the Math Library. Table 11-3 lists the math functions that are included.

TABLE 11-2: MEMORY USAGE AND PERFORMANCE

Memory Usage (bytes)[1,2]	
Code size	5250
Data size	4
Performance (cycles)[1,3]	
add	122
sub	124
mul	109
div	361
Rem	385
Sqrt	492

Note 1: Results are based on using dsPIC33F MPLAB C30 C Compiler (SW006012), version 1.20.

2: Maximum "Memory Usage" when all functions in the library are loaded. Most applications will use less.

3: Average 32-bit floating-point performance results.

TABLE 11-3: MATH FUNCTIONS

Single and Double-Precision Floating-Point Functions	
Arithmetic Functions	add, subtract, multiply, divide, remainder
Root and Power Functions	pow, sqrt
Trigonometric and Hyperbolic Functions	acos, asin, atan, atan2, cos, cosh, sin, sinh, tan, tanh
Logarithmic and Exponential Functions	exp, log, log10, frexp, ldexp
Rounding Functions	ceil, floor
Absolute Value Functions	fabs
Modular Arithmetic Functions	fmod, modf
Comparison and Conversions	comparison, integer and floating-point conversions

11.2 Peripheral Driver Library

Microchip offers a free peripheral driver library that supports the setup and control of dsPIC33F hardware peripherals, including, but not limited to:

- Analog-to-Digital Converter
- Motor Control PWM
- Quadrature Encoder Interface
- UART
- SPI™
- Data Converter Interface
- I^2C™
- General Purpose Timers
- Input Capture
- Output Compare/Simple PWM
- CAN
- I/O Ports and External Interrupts
- Reset

In addition to the hardware peripherals, the library supports software generated peripherals, such as standard LCD drivers, which support an Hitachi style controller.

The peripheral library consist of more than 270 functions, as well as several macros for simple tasks such as enabling and disabling interrupts. All peripheral driver routines are developed and optimized using the MPLAB C30 C Compiler. Electronic documentation accompanies the peripheral library to help you become familiar with and implement the library functions.

Key features of the dsPIC33F Peripheral Library include:

- A library file for each individual device from the dsPIC33F family, including functions corresponding to peripherals present in that particular device.
- 'C' `include` files that let you take advantage of predefined constants for passing parameters to various library functions. There is an `include` file for each peripheral module.
- Since the functions are in the form of precompiled libraries, they can be called from a user application program written in either MPLAB C30 C Compiler or dsPIC33F assembly language.
- Included 'C' source code allows you to customize peripheral functions to suit your specific application requirements.
- Predefined constants in the 'C' `include` files eliminate the need to refer to the details and structure of every Special Function Register while initializing peripherals or checking status bits.

11.3 DSP Algorithm Library

The free DSP library supports multiple filtering, convolution, vector and matrix functions. Among the supported functions are:

- Cascaded Infinite Impulse Response (IIR) Filters
- Correlation
- Convolution
- Finite Impulse Response (FIR) Filters
- Windowing Functions
- FFTs
- LMS Filter
- Vector Addition and Subtraction
- Vector Dot Product
- Vector Power
- Matrix Addition and Subtraction
- Matrix Multiplication

Some DSP functions use double-precision and floating-point arithmetic. All DSP routines are developed and optimized in dsPIC33F assembly language and are callable from both assembly and 'C' language. The Microchip MPLAB C30 and IAR C Compilers are supported.

Key features of the DSP Algorithm Library include:

- 49 total functions
- Full compliance with the Microchip dsPIC33F C30 C Compiler, Assembler and Linker
- Simple user interface – just one library file and one header file
- Functions are both 'C' and assembly callable
- FIR filtering functions include support for Lattice, Decimating, Interpolating and LMS filters
- IIR filtering functions include support for Canonic, Transposed Canonic and Lattice filters
- FIR and IIR functions may be used with the filter files generated by the dsPIC33F Filter Design program
- Transform functions include support for in-place and out-of-place DCT, FFT and IFFT transforms
- Window functions include support for Bartlett, Blackman, Hamming, Hanning and Kaiser windows
- Support for Program Space Visibility
- Complete function profile information including register usage, cycle count and function size information
- Electronic documentation is included to help you comprehend and use the library functions

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TABLE 11-4: FUNCTION EXECUTION TIMES

Function	Cycle Count Equation	Conditions(1)	Number of Cycles(2)	Execution Time @ 40 MIPS
Complex FFT(3)	—	N = 64	3739	93.5 µs
Complex FFT(3)	—	N = 128	8485	212.1 µs
Complex FFT(3)	—	N = 256	19055	476.4 µs
Block FIR	53 + N(4 + M)	N = 32, M = 32	1205	30.1 µs
Block FIR Lattice	41 + N(4 + 7M)	N = 32, M = 32	7337	183.4 µs
Block IIR Canonic	36 + N(8 + 7S)	N = 32, S = 4	1188	29.7 µs
Block IIR Lattice	46 + N(16 + 7M)	N = 32, M = 8	2350	58.8 µs
Matrix Add	20 + 3(C * R)	C = 8, R = 8	212	5.3 µs
Matrix Transpose	16 + C(6 + 3(R – 1))	C = 8, R = 8	232	5.8 µs
Vector Dot Product	17 + 3N	N = 32	113	2.8 µs
Vector Max	19 + 7(N – 2)	N = 32	229	5.7 µs
Vector Multiply	17 + 4N	N = 32	145	3.6 µs
Vector Power	16 + 2N	N = 32	80	2.0 µs

Note 1: C = # columns, N = # samples, M = # taps, S = # sections, R = # rows.

2: 1 cycle = 25 nanoseconds @ 40 MIPS.

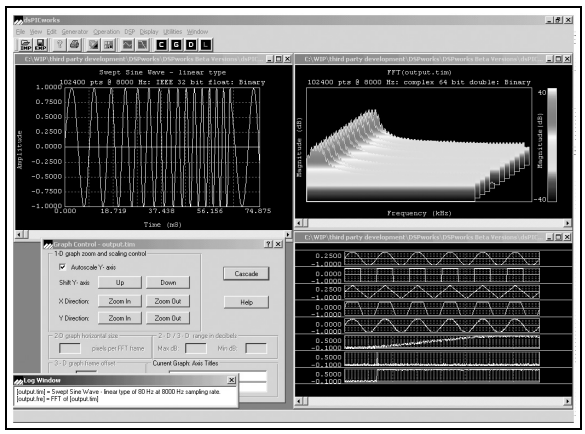
3: Complex FFT routine inherently prevents overflow.

11.4 dsPICworks™ Data Analysis and DSP Software

The dsPICworks tool is a free data analysis and signal processing package for use with Microsoft® Windows® 9x, Windows NT®, Windows 2000 and Windows XP platforms. It provides an extensive number of functions encompassing:

- Wide variety of Signal Generators – Sine, Square, Triangular, Window Functions, Noise
- Extensive DSP Functions – FFT, DCT, Filtering, Convolution, Interpolation
- Extensive Arithmetic Functions – Algebraic Expressions, Data Scaling, Clipping, etc.
- 1-D, 2-D and 3-D Displays
- Multiple Data Quantization and Saturation Options
- Multi-Channel Data Support
- Automatic “Script File”-based Execution Options available for any user-defined sequence of dsPICworks Tool Functions
- File Import/Export interoperable with MPLAB IDE
- Digital Filtering Options support Filters generated by dsPIC DSC Filter Design
- ASM30 Assembler File Option to export Data Tables into dsPIC33F RAM

FIGURE 11-1: dsPICworks™ DATA ANALYSIS AND DSP SOFTWARE



11.4.1 SIGNAL GENERATION

dsPICworks™ Data Analysis and DSP Software support an extensive set of signal generators, including basic sine, square and triangle wave generators, as well as advanced generators for window functions, unit step, unit sample, sine, exponential and noise functions. Noise, with specified distribution, can be added to any signal. Signals can be generated as 32-bit floating-point, or as 16-bit fractional fixed-point values, for any desired sampling rate. The length of the generated signal is limited only by available disk space. Signals can be imported or exported from or to MPLAB IDE file register windows. Multi-channel data can be created by a set of multiplexing functions.

11.4.2 DIGITAL SIGNAL PROCESSING (DSP) AND ARITHMETIC OPERATIONS

dsPICworks Data Analysis and DSP Software have a wide range of DSP and arithmetic functions that can be applied to signals. Standard DSP functions include transform operations: FFT and DCT, convolution and correlation, signal decimation, signal interpolation sample rate conversion and digital filtering. Digital filtering is an important part of the dsPICworks tool. It uses filters designed by the sister-application, dsPIC DSC Filter Design, and applies them to synthesized or imported signals. The dsPICworks tool also features special operations, such as signal clipping, scaling and quantization, all of which are vital in real practical analysis of DSP algorithms.

11.4.3 DISPLAY AND MEASUREMENT

dsPICworks Data Analysis and DSP Software have a wide variety of display and measurement options. Frequency domain data may be plotted in the form of 2-dimensional ‘spectrogram’ and 3-dimensional ‘waterfall’ options. The signals can be measured accurately by a simple mouse click. The log window shows current cursor coordinates, as well as derived values, such as the difference from last position and signal frequency. Signal strength can be measured over a particular range of frequencies. Special support also exists for displaying multi-channel and multiplexed data. Graphs allow zoom options. The user can choose from a set of color scheme options to customize display settings.

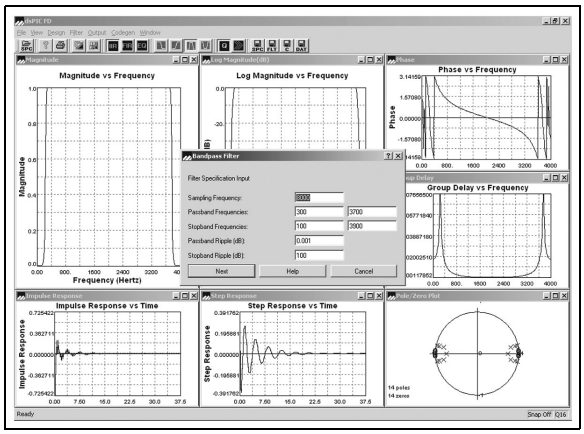
11.4.4 FILE IMPORT/EXPORT – MPLAB IDE AND MPLAB ASM30 SUPPORT

dsPICworks Data Analysis and DSP Software allow data to be imported from the external world in the form of ASCII text or binary files. Conversely, it also allows data to be exported out in the form of files. The dsPICworks tool supports all file formats supported by the MPLAB import/export table. This feature allows the user to bring real-world data from MPLAB IDE into the dsPICworks tool for analysis. The dsPICworks tool can also create ASM30 assembler files that can be included into the MPLAB workspace.

11.5 Digital Filter Design Software Utility

The Digital Filter Design tool for the dsPIC33F 16-bit digital signal controllers makes designing, analyzing and implementing Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) digital filters easy through a menu-driven, user-intuitive interface. This tool performs complex mathematical computations for filter design, provides superior graphical displays and generates comprehensive design reports. Desired filter frequency specifications are entered and the tool automatically generates the filter code and coefficient files ready to use in the MPLAB Integrated Development Environment (IDE). System analysis of the filter transfer function is supported with multiple generated graphs, such as magnitude, phase, group delay, log magnitude, impulse response and pole/zero locations.

FIGURE 11-2: DIGITAL FILTER DESIGN TOOL INTERFACE



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Key features of the Digital Filter Design tool include:

Finite Impulse Response Filter Design

- Design Method Selection
  - FIR Windows Design
  - FIR Equiripple Design (Parks-McClellan)
- Low-Pass, High-Pass, Band-Pass and Band-Stop Filters
- FIR Filters can have up to 513 taps
- The following window functions are supported:
  - Rectangular
  - Hanning (Hann)
  - Hamming
  - Triangular
  - Blackman
  - Exact Blackman
  - 3 Term Cosine
  - 3 Term Cosine with Continuous 3rd Derivative
  - Minimum 3 Term Cosine
  - 4 Term Cosine
  - 4 Term Cosine with continuous 5th Derivative
  - Minimum 4 Term Cosine
  - Good 4 Term Blackman Harris
  - Harris Flat Top
  - Kaiser
  - Dolph-Tschebyscheff
  - Taylor
  - Gaussian
- Reports show design details, such as window coefficients and impulse response prior to multiplying by the window function

Infinite Impulse Response Filter Design

- Low-Pass, High-Pass, Band-Pass and Band-Stop Filters
- Filter Orders up to 10 for Low-Pass and High-Pass Filters
- Filter Orders up to 20 for Band-Pass and Band-Stop Filters
- Five Analog Prototype Filters are available:
  - Butterworth
  - Tschebyscheff
  - Inverse Tschebyscheff
  - Elliptic
  - Bessel
- Digital Transformations are performed by Bilinear Transformation Method
- Reports show design details, such as all transformations from normalized low-pass filter to desired filter

Code Generation Features

- Generated files are compliant with the Microchip dsPIC33F C30 C Compiler, Assembler and Linker
- Choice of placement of coefficients in Program Space or Data Space
- 'C' Wrapper/Header Code Generation

Graphs

- Magnitude Response vs. Frequency
- Log Magnitude vs. Frequency
- Phase Response vs. Frequency
- Group Delay vs. Frequency
- Impulse Response vs. Time (per sample)
- Step Response vs. Time (per sample)
- Pole and Zero Locations (IIR only)

11.6 Microchip TCP/IP Stack

The free Microchip TCP/IP Stack is a suite of programs that can provide services to standard (HTTP Server, Mail Client, etc.) or custom TCP/IP-based applications. Users do not need to be an expert in TCP/IP specifications to use it and only need specific knowledge of TCP/IP in the accompanying HTTP Server application.

This stack is implemented in a modular fashion, with all of its services creating highly abstracted layers, each layer accessing services from one or more layers directly below it. The stack is optimized for size and is designed to run on the dsPIC33F using the dsPICDEM.net™ Development Board; however, it can be easily retargeted to any hardware equipped with a dsPIC33F. HTML web pages generated by the dsPIC33F can be viewed with a standard web browser such as Microsoft Internet Explorer.

Key features of the Microchip TCP/IP Stack include:

- Out-of-box support for Microchip C30 C Compiler
- Implements complete TCP state machine
- Multiple TCP and UDP sockets with simultaneous connection/management
- Includes modules supporting various standard protocols: MAC, SLIP, ARP, IP, ICMP, TCP, SNMP, UDP, DHCP, FTP, IP Gleaning, HTTP, MPFS (Microchip File System)
- Can be used as a part of the HTTP Server (included) or any custom TCP/IP-based application
- RTOS independent

11.7 Soft Modem Library

The Microchip data modem library is composed of ITU-T compliant algorithms for V.21, V.22, V.22bis, V.23, V.32 and V.32bis modem recommendations. Bell standard 103 is also included in this library.

V.21, V.23 and Bell 103 are Frequency Shift Keying (FSK) modems. V.32, V.32bis and V.22bis are Quadrature Amplitude Modulation (QAM) modems. V.22 is a Quadrature Phase Shift Keying (QPSK) modem. V.21, V.22, V.22bis, V.32 and V.32bis are all 2-wire, full-duplex modems. V.23 is a full-duplex modem when it operates with a 75 bps backwards channel.

V.22bis includes fallback to V.22, V.23 and V.21 standards. V.32bis optionally falls back to V.22bis, V.22 and V.21 standards.

The dsPIC DSC Soft Modem is well-suited for small transaction oriented applications, such as, but not limited to:

- POS Terminals
- Set Top Boxes
- Drop Boxes
- Fire Panels
- Internet Enabled Home Security Systems
- Internet Connected Power, Gas and Water Meters
- Internet Connected Vending Machines
- Smart Appliances
- Industrial Monitoring

Functions supporting ITU-T Recommendation V.42 are provided with each library. V.42 contains a High-Level Data Link Control (HDLC) protocol, referred to as Link Access Procedure for Modems (LAPM) and defines error correcting protocols for modems.

All data pump modulation and demodulation functions are written in ASM30 assembly code yielding optimal code size and execution time. The AT, V.42 and data pump APIs are written in C30 C Compiler language.

Electronic documentation accompanies the modem library to help you become familiar with and implement the library functions. A comprehensive *"dsPIC30F Soft Modem Library User's Guide"* describes the required APIs for the AT, V.42 and data pump layers.

11.8 Speech Recognition Library

The dsPIC Speech Recognition Library provides voice control of embedded applications that require an alternative user interface. With a vocabulary of up to 100 words, the Speech Recognition Library allows users to control their application using spoken commands. The Speech Recognition Library is an ideal front end for hands-free products, such as modem appliances, security panels and cell phones. The Speech Recognition Library has very modest memory and processing requirements and is targeted for the dsPIC30F5011, dsPIC30F5013, dsPIC30F6012 and dsPIC30F6014 processors.

Key features of the dsPIC DSC Speech Recognition Library include:

- US English language support
- Speaker independent recognition of isolated words
- No speaker training is required
- Hidden Markov Modem-based recognition system
- Recognition time < 500 msec
- Master library of 100 common words (listed in the *"dsPIC30F Speech Recognition Library User's Guide"*)
- Windows operating system-based utility allows the user to create a custom word library from the master library
- Additional words can be added to the master library (fee based)
- Data tables can be stored in external memory
- Optional keyword activation and silence detection
- Optional system self-test using a predefined keyword
- Flexible API
- Full compliance with Microchip MPLAB C30 C Compiler Language Tools
- *"dsPIC30F Speech Recognition Library User's Guide"* and *"dsPIC30F Word Library Builder User's Guide"*
- Designed to run on dsPICDEM™ 1.1 General Purpose Development Board (DM300014)

11.8.1 RESOURCE REQUIREMENTS

- Sampling Interface: Si-3000 Audio Codec operating at 12.0 kHz
- System Operating Frequency: 12.288, 18.432 or 24.576 MHz
- Computational Power: 8 MIPS
- Program Flash Memory: 18 KB + 1.5 KB for each library word
- RAM: < 3.0 KB

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11.9 Noise Suppression Library

The dsPIC DSC Noise Suppression Library provides a function to suppress the effect of noise interfering with a speech signal. This function is useful for microphone-based applications which have a potential for incoming speech getting corrupted by ambient noise captured by a microphone. It is especially suitable for systems in which an acoustically isolated noise reference is not available, such as:

- Hands-Free Cell Phone Kits
- Speakerphones
- Intercoms
- Teleconferencing Systems
- Headsets
- As a front end to a Speech Recognition or Speech Encoding system
- Any microphone-based application that needs to eliminate undesired noise
- Any application that needs to eliminate noise interference from signals received over a communication channel

The Noise Suppression Library uses an 8 kHz sampling rate. However, the library includes sample rate conversion functions that ensure interoperability with libraries and speech sampling peripherals configured for higher sampling rates (9.6 kHz, 11.025 kHz or 12 kHz).

Key features of the Noise Suppression Library include:

- All functions can be called from either a 'C' or assembly application program
- Full compliance with the Microchip C30 C Compiler, Assembler and Linker
- Precompiled library archive files
- Highly optimized assembly code, utilizing DSP instructions and advanced addressing modes
- Audio Bandwidth: 0-4 kHz at 8 kHz sampling rate
- 10-20 dB noise reduction depending on type of noise
- *"dsPIC30F Noise Suppression Library User's Guide"*
- Demo application source code is provided
- Accessory Kit available for purchase includes: audio cable, headset, oscillators, microphone, speaker, DB9 M/F RS-232 cable, DB9M-DB9M null modem adapter and can be used for library evaluation

TABLE 11-5: RESOURCE REQUIREMENTS

Algorithm	MIPS	Flash	RAM
Noise Suppression	3.3	7 KB	1 KB
Sample Rate Conversion	1.0	2.6 KB	0.5 KB

Note: The user application might require an additional 1 KB-1.5 KB for data buffering (application-dependent).

11.10 Acoustic Echo Cancellation Library

The Acoustic Echo Cancellation (AEC) Library provides a function to eliminate echo generated in the acoustic path between a speaker and a microphone. This function is useful for speech and telephony applications in which a speaker and a microphone are located in close proximity to each other and therefore, susceptible to signals propagating from the speaker to the microphone resulting in a perceptible and distracting echo effect at the far end. It is especially suitable for these applications:

- Hands-Free Cell Phone Kits
- Speakerphones
- Intercoms
- Teleconferencing Systems

For hands-free phones intended to be used in compact environments, such as a car cabin, this library is fully compliant with the G.167 standard for Acoustic Echo Cancellation.

Like the Noise Suppression Library, the Acoustic Echo Cancellation Library also includes sample rate conversion functions.

Key features of the AEC Library include:

- All functions can be called from either a 'C' or assembly application program
- Full compliance with the Microchip C30 C Compiler, Assembler and Linker
- Precompiled library archive files
- Highly optimized assembly code, utilizing DSP instructions and advanced addressing modes
- Echo cancellation for 16, 32 or 64 ms echo delay or 'tail length' (configurable)
- Fully tested for compliance with G.167 specifications for in-car applications
- Audio Bandwidth: 0-4 kHz at 8 kHz sampling rate
- Convergence Rate: up to 43 dB/sec., typically > 30 dB/sec.
- Echo Cancellation: Up to 50 dB, typically > 40 dB
- *"dsPIC30F Acoustic Echo Cancellation Library User's Guide"*
- Demo application source code is provided
- Accessory Kit available for purchase

TABLE 11-6: RESOURCE REQUIREMENTS

Algorithm	MIPS	Flash	RAM
AEC – 64 ms Echo Tail	16.5	6 KB	5.7 KB
AEC – 32 ms Echo Tail	10.5	6 KB	3.4 KB
AEC – 16 ms Echo Tail	7.5	6 KB	2.6 KB
Sample Rate Conversion	1.0	2.6 KB	0.5 KB

Note: The user application might require an additional 2 KB-2.5 KB for data buffering (application-dependent).

11.11 Symmetric Key Embedded Encryption Library

Microchip offers a reliable security solution for embedded applications built on the dsPIC33F platform. This solution is provided by means of two libraries – Symmetric Key and Asymmetric Key Embedded Encryption Libraries. The Symmetric Key Library includes the following:

- Hash functions
  - SHA-1 Secure Hash Standard
  - MD5 Message Digest
- Symmetric Key Encryption/Decryption functions
  - Advanced Encryption Standard (AES)
  - Triple Data Encryption Standard (Triple-DES)
- Random Number Generator functions
  - Deterministic Random Bit Generator ANSI X9.82

Some typical applications for this library include:

- Mobile and Wireless Devices, PDAs
- Secure Banking
- Secure Web Transactions
  - Secure Socket Layer (SSL)
  - Transport Layer Security (TLS)
  - Secure Multipurpose Mail Extensions (S/MIME)
- ZigBee™ Technology and other Monitoring and Control Applications
- Smart Card Readers/Trusted Card Readers
- Friend/Foe Identification
- Secure devices and peripherals interoperating with TCG (Trusted Computing Group) and NGSCB (Microsoft Next Generation Secure Computing Base) personal computers

Key features of the Symmetric Key Embedded Encryption Library include:

- C-callable library functions developed in MPLAB ASM30 assembly language
- Optimized for speed, code size and RAM usage
  - RAM usage below 60 bytes
- Library functions extensively tested for adherence to applicable standards
- Symmetric Key Encryption/Decryption functions support multiple modes of operation:
  - Electronic Code Book (ECB) mode
  - Cipher Block Chaining with Message Authentication (CBC-MAC) mode
  - Counter (CTR) mode
  - Combined CBC-MAC and CTR (CCM) mode
- *"dsPIC30F Embedded Encryption Libraries User's Guide"*
- Several examples of use are provided for each library function

11.12 Asymmetric Key Embedded Encryption Library

Microchip offers a reliable security solution for embedded applications built on the dsPIC33F platform. This solution is provided by means of two libraries – Symmetric Key and Asymmetric Key Embedded Encryption Libraries. The Asymmetric Key Library includes the following:

- Public Key Encryption/Decryption functions
  - RSA (1024 and 2048-bit)
- Key Agreement Protocol
  - Diffie-Hellman (1024 and 2048-bit)
- Signing and Verification
  - DSA (1024-bit)
  - RSA (1024 and 2048-bit)
- Hash functions
  - SHA-1 Secure Hash Standard
  - MD5 Message Digest
- Random Number Generator functions
  - ANSI X9.82

Some typical applications for this library include:

- Mobile and Wireless Devices, PDAs
- Secure Banking
- Secure Web Transactions
  - Secure Socket Layer (SSL)
  - Transport Layer Security (TLS)
  - Secure Multipurpose Mail Extensions (S/MIME)
- ZigBee Technology and other Monitoring and Control Applications
- Smart Card Readers/Trusted Card Readers
- Friend/Foe Identification
- Secure devices and peripherals interoperating with TCG (Trusted Computing Group) and NGSCB (Microsoft Next Generation Secure Computing Base) personal computers

Key features of the Asymmetric Key Embedded Encryption Library include:

- C-callable library functions developed in MPLAB ASM30 assembly language
- Optimized for speed, code size and RAM usage
  - RAM usage below 100 bytes
- Library functions extensively tested for adherence to applicable standards
- *"dsPIC30F Embedded Encryption Libraries User's Guide"*
- Several examples of use are provided for each library function

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11.13 Speech Encoding/Decoding Library

The Speech Encoding/Decoding Library performs toll-quality voice compression and voice decompression. The library is based on a modified version of the Speex speech encoder/decoder source code and features a 16:1 compression ratio. It samples speech at 8 kHz and compresses it to a data rate of 8 kbps. Storing compressed speech for playback requires approximately 1 KB of memory for each second of speech. The library is especially suitable for the following voice-based applications:

- Answering Machines
- Building and Home Safety Systems
- Intercoms
- Smart Appliances
- Voice Recorders
- Walkie-Talkies
- Any Application using Message Playback

A PC-based speech encoder utility program allows you to create your own encoded speech files for playback. Encoded speech files are made from either a PC microphone or existing WAV file. Once you create the encoded speech files, they are added to your MPLAB C30 project, just like a regular source file, and built into your application. The speech encoder utility allows you to select four target memory areas to store your speech file: program Flash memory, RAM and external Flash memory. External Flash memory allows you to store many minutes of speech (1 minute of speech requires 60 KB) and it is supported through a general purpose I/O port.

Key features of the Speech Encoding/Decoding Library include:

- PESQ-based Mean Opinion Score: 3.7-4.2 (out of 5.0)
- Code Excited Linear Prediction (CELP) based coding
- 2 Analog Input Interfaces – codec or on-chip ADC
- 2 Analog Output Interfaces – codec or on-chip PWM
- Optional Voice Activity Detection
- Storing compressed speech requires 1 KB of memory per second of speech
- Royalty-free (only one-time license fee)
- Full compliance with Microchip MPLAB C30 C Compiler Language Tools
- *"dsPIC30F Speech Encoding/Decoding Library User's Guide"*
- Designed to run on dsPICDEM 1.1 General Purpose Development Board (DM300014)

12.0 THIRD PARTY DEVELOPMENT TOOLS AND APPLICATION LIBRARIES

Besides providing development tools and application libraries for dsPIC33F products, Microchip also partners with key third party tool manufacturers to develop quality hardware and software tools in support of the dsPIC33F product family. Details of various third party development tools will be provided shortly.

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13.0 dsPIC33F HARDWARE DEVELOPMENT BOARDS

Microchip initially offers two hardware development boards that help you quickly prototype and validate key aspects of your design. Each board features various dsPIC33F peripherals and supports Microchip's MPLAB In-Circuit Debugger (ICD 2) tool for cost-effective debugging and programming of the dsPIC33F devices. These two boards are shown in Table 13-1.

Microchip plans to offer additional hardware development boards to support the dsPIC33F product family. Contact Microchip DSCD Marketing for additional information.

TABLE 13-1: HARDWARE DEVELOPMENT BOARDS

	Development Tool	Description	Part #	From
Development Boards and Reference Designs	**General Purpose Development Board**	dsPICDEM™ 80-Pin Starter Development Board	DM300019	Microchip
		Explorer 16 Development Board	DM240001	Microchip
Plug-in Samples	**Plug-in Sample** (see **Section 13.3 Plug-in Modules**)	PC board with 80-pin dsPIC30F6014A general purpose MCU sample; use with DM300019 development board.	MA300014	Microchip
		PC board with 100-pin dsPIC33F MCU sample; use with DM240001 development board.	MA330011	Microchip
		PC board with 100-pin dsPIC33F MCU sample; use with DM300019 development board.	MA330012	Microchip
Accessory Kits	**Acoustic Accessory Kit** (see **Section 13.3 Plug-in Modules**)	Accessory Kit includes: audio cable, headset, oscillators, microphone, speaker, DB9 M/F RS-232 cable, DB9M-DB9M Null Modem Adapter and can be used for library evaluation.	AC300030	Microchip

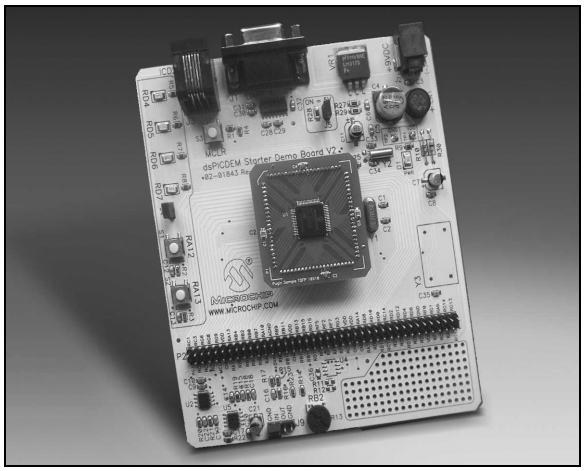
13.1 dsPICDEM™ 80-Pin Starter Development Board

This development board offers a very economical way to evaluate both the dsPIC30F and dsPIC33F General Purpose and Motor Control Family devices. This board is an ideal prototyping tool to help you quickly develop and validate key design requirements.

Some key features and attributes of the dsPICDEM 80-Pin Starter Development Board include:

- Includes an 80-pin dsPIC30F6014A plug-in module (MA300014)
- Power input from 9V supply
- Selectable voltage regulator outputs of 5V and 3.3V
- LEDs, switches, potentiometer, UART interface
- A/D input filter circuit for speech band signal input
- On-board DAC and filter for speech band signal output
- Circuit prototyping area
- Assembly language demonstration program and tutorial
- Can accommodate 80-pin dsPIC30F6010 plug-in module (MA300013)
- Can accommodate 100 to 80-pin adapter dsPIC33F plug-in module (MA330012)

FIGURE 13-1: dsPICDEM™ 80-PIN STARTER DEVELOPMENT BOARD



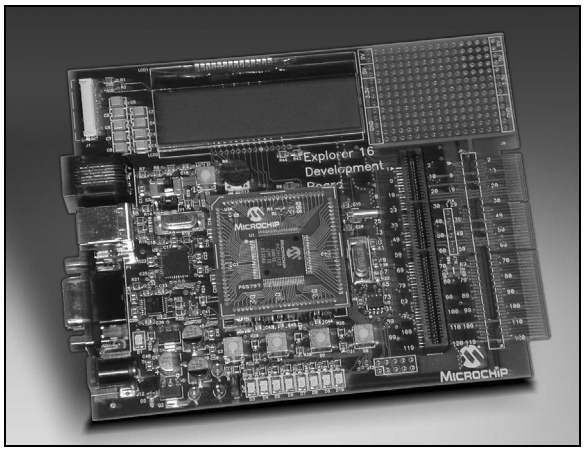
13.2 Explorer 16 Development Board

This development board offers a very economical way to evaluate both the dsPIC33F General Purpose and Motor Control Family devices, as well as the PIC24F devices. This board is an ideal prototyping tool to help you quickly develop and validate key design requirements.

Some key features and attributes of the Explorer 16 Development Board include:

- Includes a 100-pin dsPIC33F plug-in module (MA330011)
- Includes a 100-pin PIC24 plug-in module (part # TBD)
- Power input from 9V supply
- Modular design for plug-in demonstration boards, expansion header
- ICD 2 and JTAG connection for reprogramming
- USB and protocol translation support through PIC18F4450
- RS-232 connection with firmware and driver support
- LED bank for general indication
- Serial EEPROM
- 16 x 2 alphanumeric LCD
- Temperature sensor
- Terminal interface program and menu programs

FIGURE 13-2: EXPLORER 16 DEVELOPMENT BOARD



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13.3 Plug-in Modules

The various dsPIC33F development boards may use the plug-in modules for the dsPIC33F silicon devices. Since the boards contain device header pins on the PCB, they also are used to provide flexibility for the replacement of the dsPIC33F silicon. Three different plug-in sample types will be provided, supporting the 64-pin, 80-pin and 100-pin TQFP package types for General Purpose and Motor Control Family device samples. The use of plug-in samples is considered to be an interim development board mechanization.

13.4 Acoustic Accessory Kit

The Acoustic Accessory Kit includes the following accessories targeted towards acoustics-oriented library (NS, AEC, etc.) evaluation and application development support:

- 6 ft. Stereo Audio Cable
- Stereo Headset
- Two 14.7456 MHz Oscillators
- Clip-on Microphone
- Fold-up Speaker
- 6 ft. DB9 M/F RS-232 Cable
- DB9M-DB9M Null Modem Adapter

APPENDIX A: DEVICE I/O PINOUTS AND FUNCTIONS FOR GENERAL PURPOSE FAMILY

Table A-1 provides a brief description of device I/O pinouts and functions that can be multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE A-1: PINOUT I/O DESCRIPTIONS FOR GENERAL PURPOSE FAMILY

Pin Name	Pin Type	Input Buffer Type	Description
AN0-AN23	I	Analog	Analog input channels.
AVDD	P	P	Positive supply for analog module.
AVSS	P	P	Ground reference for analog module.
CLKI	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
COFS	I/O	ST	Data Converter Interface frame synchronization pin.
CSCK	I/O	ST	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Data Converter Interface serial data input pin.
CSDO	O	—	Data Converter Interface serial data output pin.
C1RX	I	ST	ECAN1 bus receive pin.
C1TX	O	—	ECAN1 bus transmit pin.
C2RX	I	ST	ECAN2 bus receive pin.
C2TX	O	—	ECAN2 bus transmit pin.
PGD1/EMUD1	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGC1/EMUC1	I	ST	Clock input pin for programming/debugging communication channel 1.
PGD2/EMUD2	I/O	ST	Data I/O pin for programming/debugging communication channel 2.
PGC2/EMUC2	I	ST	Clock input pin for programming/debugging communication channel 2.
PGD3/EMUD3	I/O	ST	Data I/O pin for programming/debugging communication channel 3.
PGC3/EMUC3	I	ST	Clock input pin for programming/debugging communication channel 3.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INT0	I	ST	External interrupt 0.
INT1	I	ST	External interrupt 1.
INT2	I	ST	External interrupt 2.
INT3	I	ST	External interrupt 3.
INT4	I	ST	External interrupt 4.
$\overline{MCLR}$	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active-low Reset to the device.
OCFA	I	ST	Compare Fault A input (for Compare Channels 1, 2, 3 and 4).
OCFB	I	ST	Compare Fault B input (for Compare Channels 5, 6, 7 and 8).
OC1-OC8	O	—	Compare outputs 1 through 8.
OSC1	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
RA0-RA7	I/O	ST	PORTA is a bidirectional I/O port.
RA9-RA10	I/O	ST	
RA12-RA15	I/O	ST	
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; P = Power

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TABLE A-1: PINOUT I/O DESCRIPTIONS FOR GENERAL PURPOSE FAMILY (CONTINUED)

Pin Name	Pin Type	Input Buffer Type	Description
RC1-RC4 RC12-RC15	I/O I/O	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8 RF12-RF13	I/O I/O	ST ST	PORTF is a bidirectional I/O port.
RG0-RG3 RG6-RG9 RG12-RG15	I/O I/O I/O	ST ST ST	PORTG is a bidirectional I/O port.
SCK1 SDI1 SDO1 $\overline{SS1}$ SCK2 SDI2 SDO2 $\overline{SS2}$	I/O I O I I/O I O I	ST ST — ST ST ST — ST	Synchronous serial clock input/output for SPI1. SPI1 data in. SPI1 data out. SPI1 slave synchronization. Synchronous serial clock input/output for SPI2. SPI2 data in. SPI2 data out. SPI2 slave synchronization.
SCL1 SDA1 SCL2 SDA2	I/O I/O I/O I/O	ST ST ST ST	Synchronous serial clock input/output for I2C1. Synchronous serial data input/output for I2C1. Synchronous serial clock input/output for I2C2. Synchronous serial data input/output for I2C2.
SOSCI SOSCO	I O	ST/CMOS —	32 kHz low-power oscillator crystal input; CMOS otherwise. 32 kHz low-power oscillator crystal output.
TMS TCK TDI TDO	I I/O I O	ST ST ST —	JTAG Test mode select pin. JTAG test clock input/output pin. JTAG test data input pin. JTAG test data output pin.
T1CK T2CK T3CK T4CK T5CK T6CK T7CK T8CK T9CK	I I I I I I I I I	ST ST ST ST ST ST ST ST ST	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input. Timer6 external clock input. Timer7 external clock input. Timer8 external clock input. Timer9 external clock input.
U1CTS U1RTS U1RX U1TX U2CTS U2RTS U2RX U2TX	I O I O I O I O	ST — ST — ST — ST —	UART1 clear to send. UART1 ready to send. UART1 receive. UART1 transmit. UART2 clear to send. UART2 ready to send. UART2 receive. UART2 transmit.
V_{DD}	P	—	Positive supply for peripheral logic and I/O pins.
V_{DDCORE}	P	—	CPU logic filter capacitor connection.
V_{SS}	P	—	Ground reference for logic and I/O pins.
V_{REF+}	I	Analog	Analog voltage reference (high) input.
V_{REF-}	I	Analog	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; P = Power

TABLE A-2: dsPIC33F GENERAL PURPOSE FAMILY VARIANTS (DEVICES MARKED "PS")

Device	Pins	Program Flash Memory (KB)	RAM (KB)(1)	Timer 16-bit	Input Capture	Output Compare Std. PWM	Codec Interface	A/D Converter	UART	SPI™	I²C™	CAN	I/O Pins (Max)(2)	Packages
33FJ128GP706	64	128	17	9	8	8	1	2 A/D, 18 ch	2	2	2	2	53	PT
33FJ128GP708	80	128	17	9	8	8	1	2 A/D, 24 ch	2	2	2	2	69	PT
33FJ256GP710	100	256	33	9	8	8	1	2 A/D, 32 ch	2	2	2	2	86	PF

Note 1: RAM size is inclusive of 1 KB DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

Note: Prototype samples are intended for dsPIC33F early adopters and are based on early revision silicon. Devices are marked with "PS" suffix. Major differences are noted in this data sheet. For additional information, please refer to the *"dsPIC33F Data Sheet"*.

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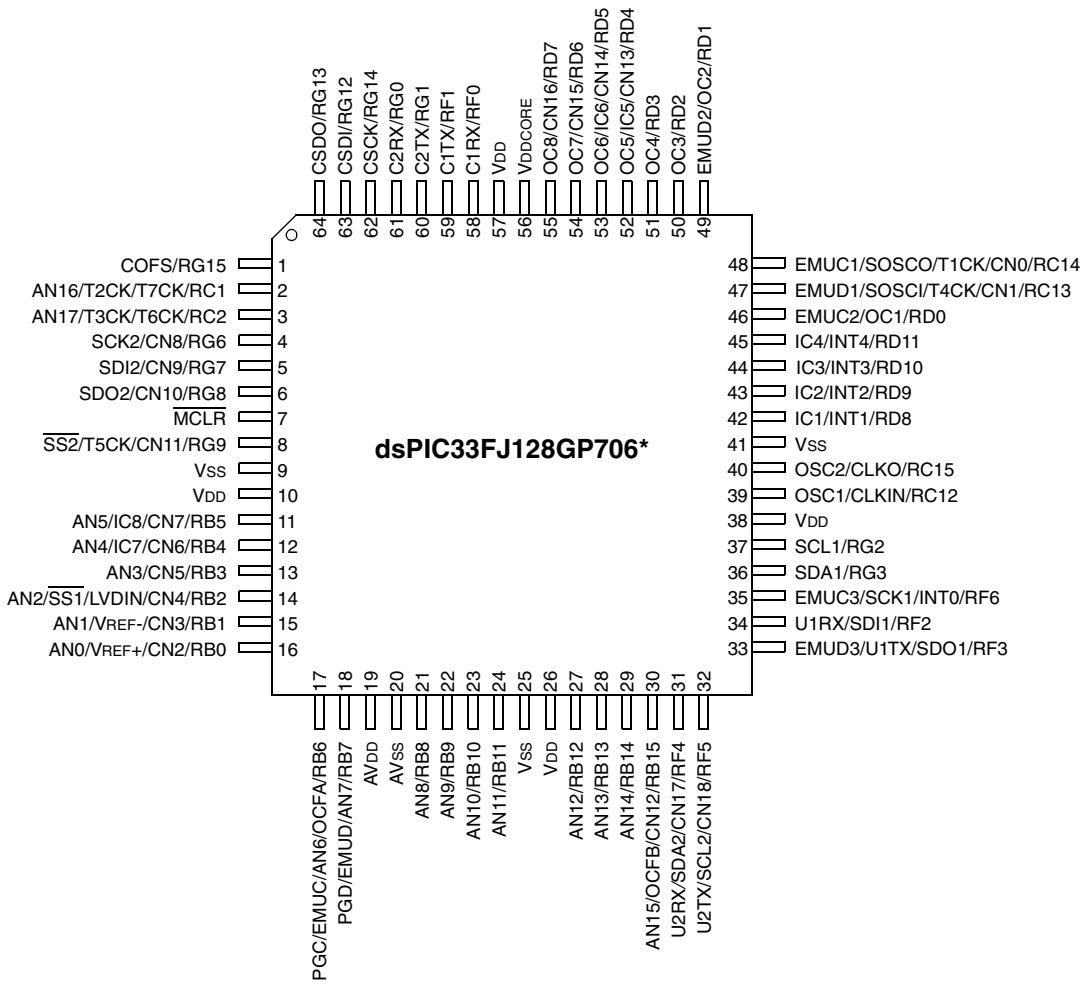
Pin Diagrams

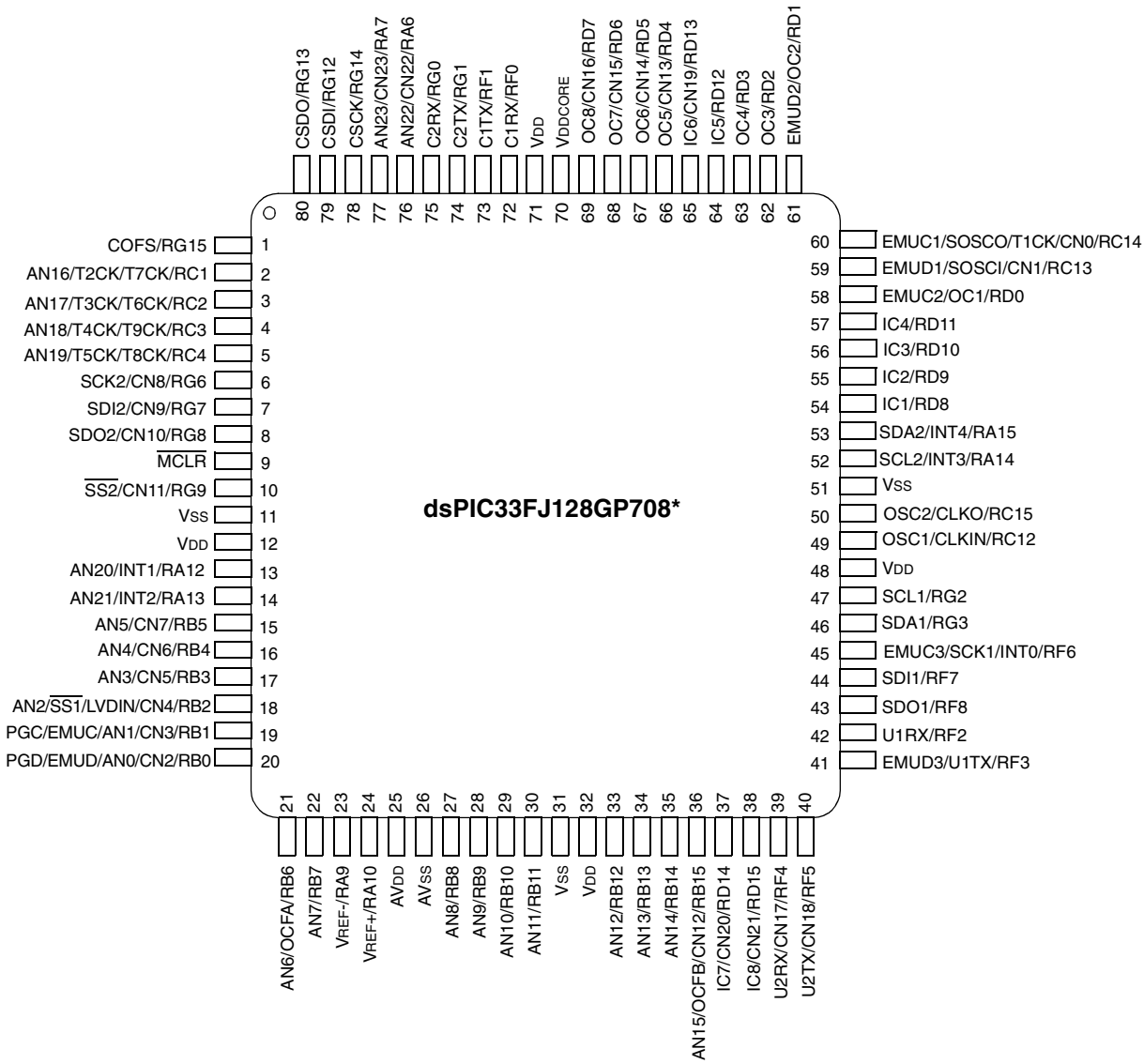
64-Pin TQFP



*Device is marked with ‘PS’ designator.

Pin Diagrams (Continued)

80-Pin TQFP



*Device is marked with 'PS' designator.

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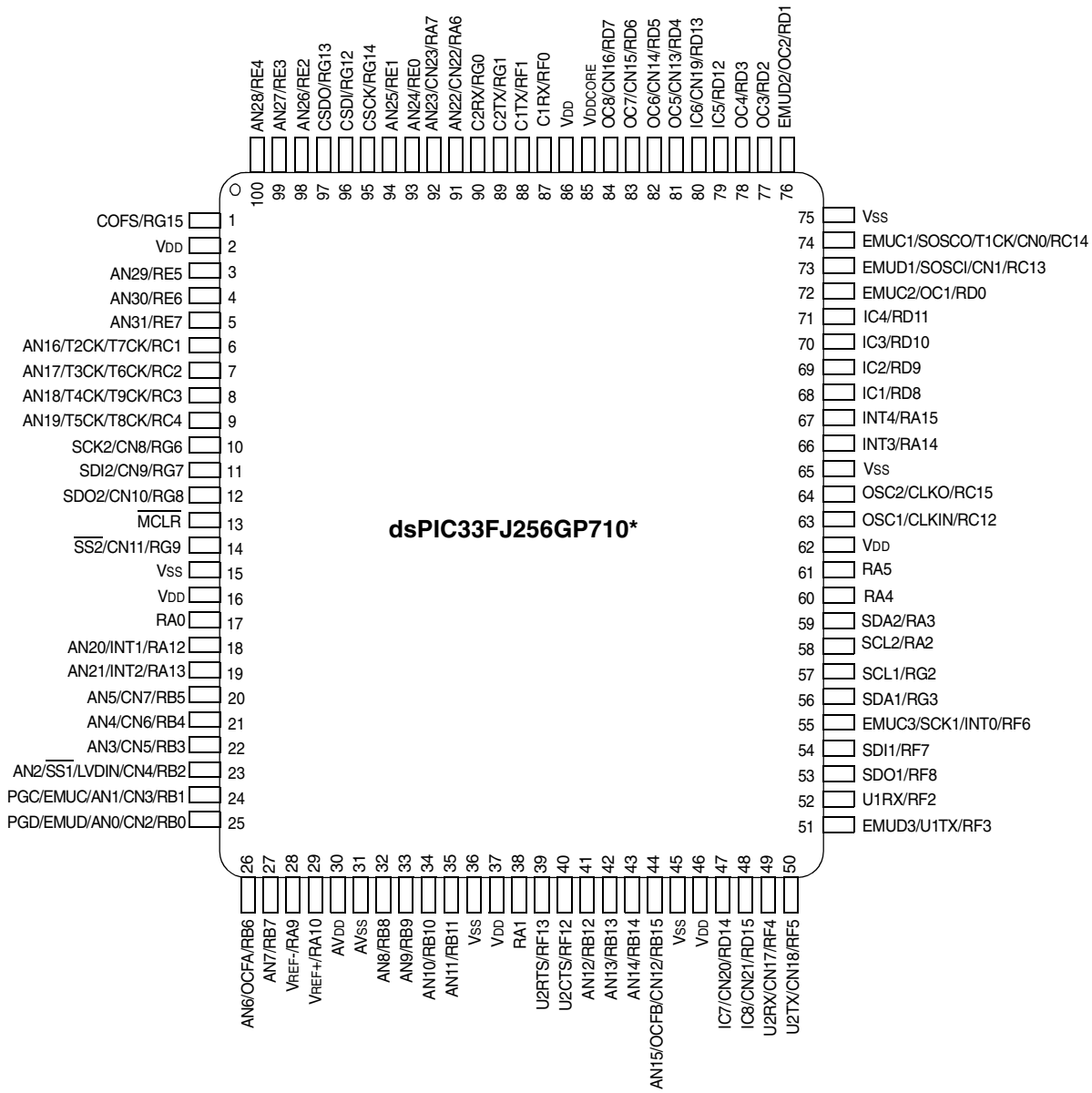
Pin Diagrams (Continued)

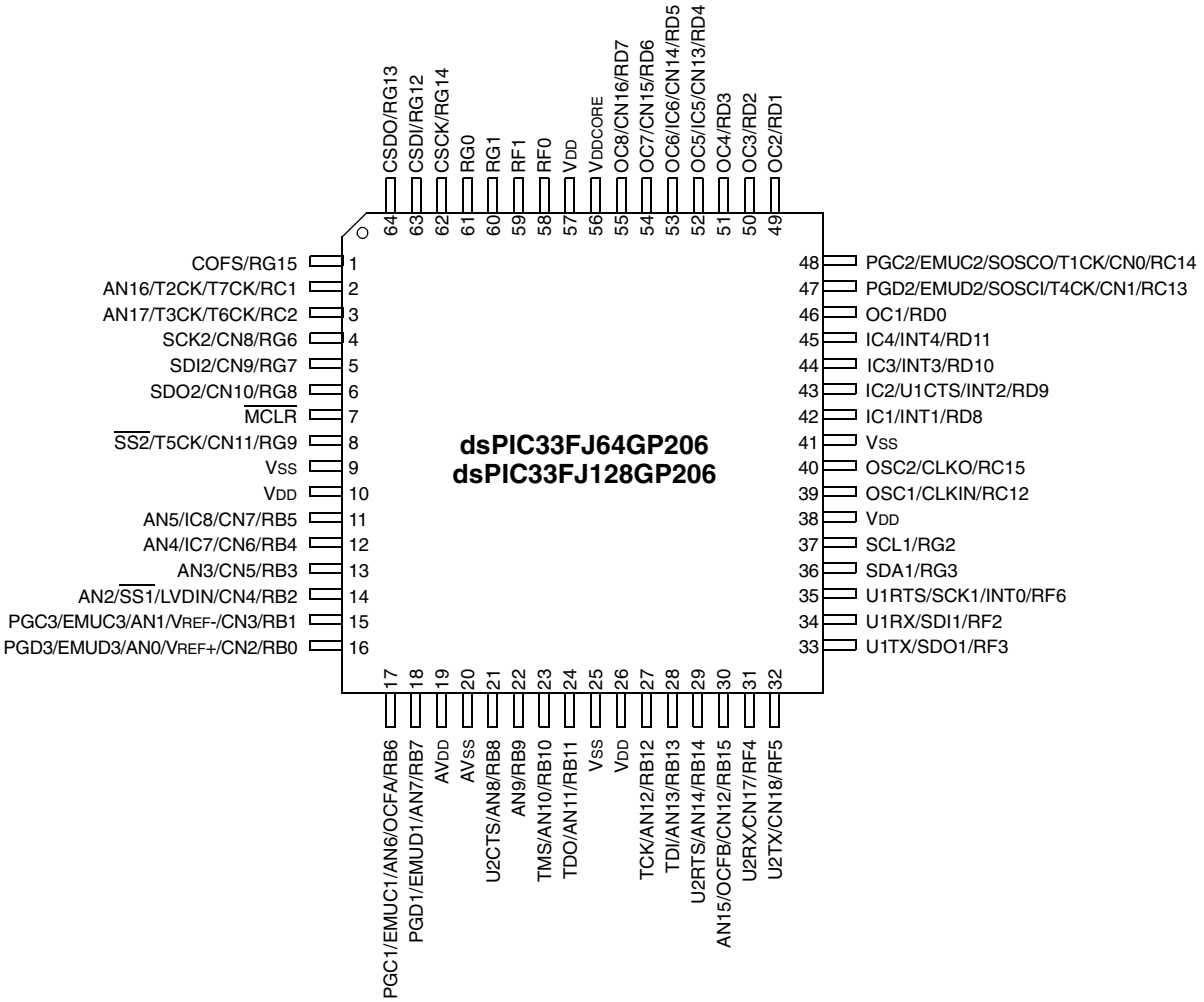
100-Pin TQFP



*Device is marked with 'PS' designator.

Pin Diagrams (Continued)

64-Pin TQFP



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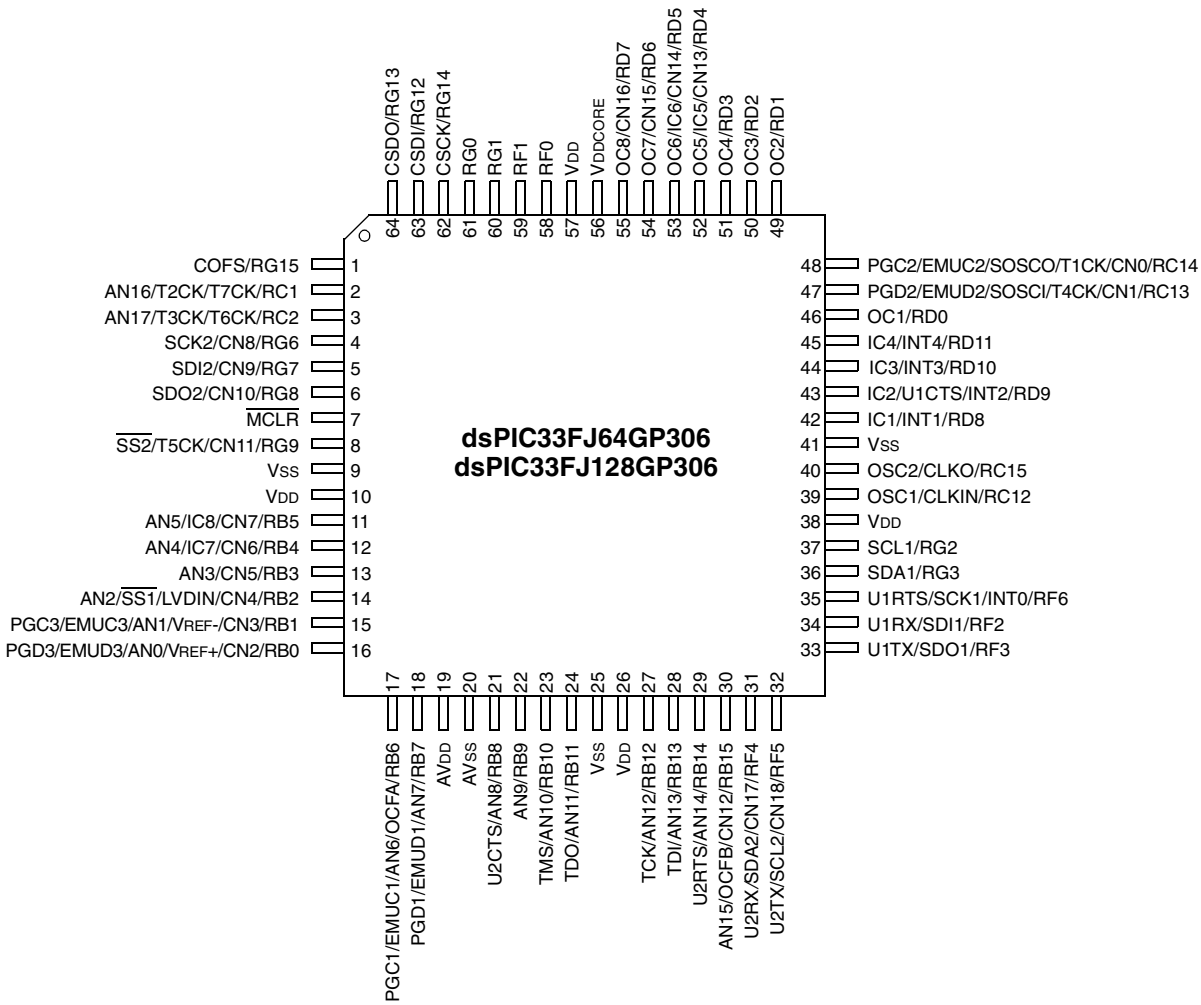
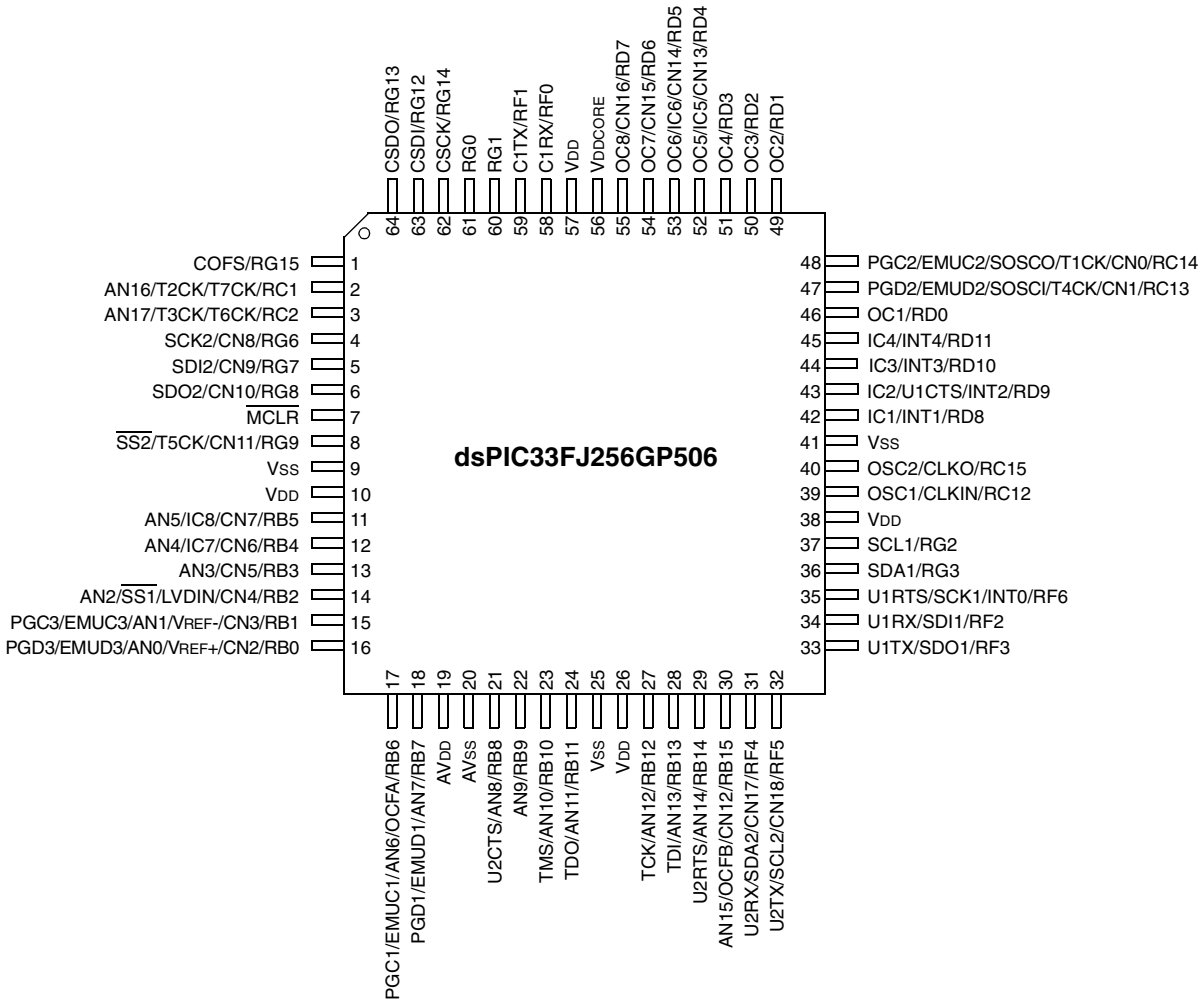
Pin Diagrams (Continued)

64-Pin TQFP



Pin Diagrams (Continued)

64-Pin TQFP



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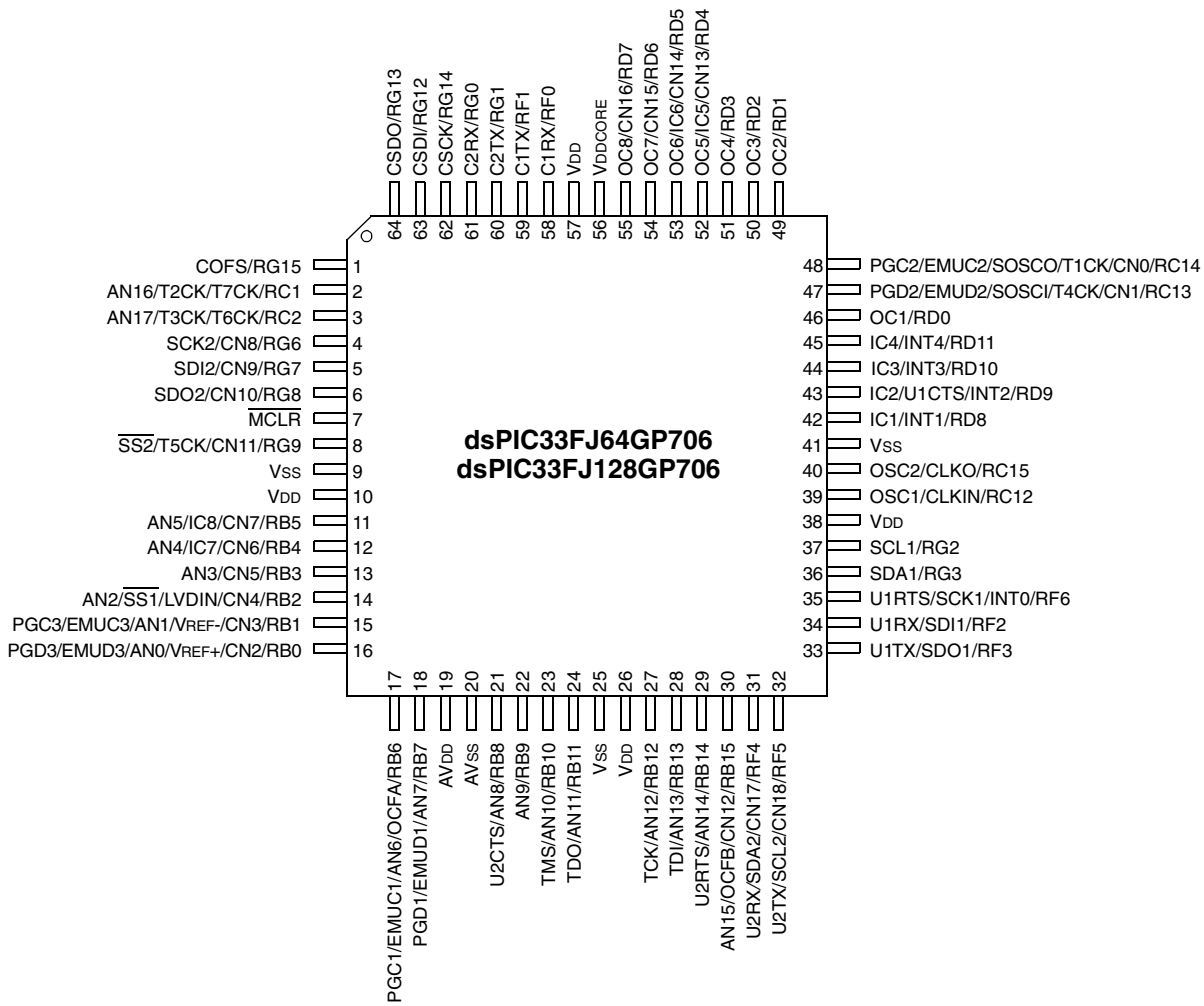
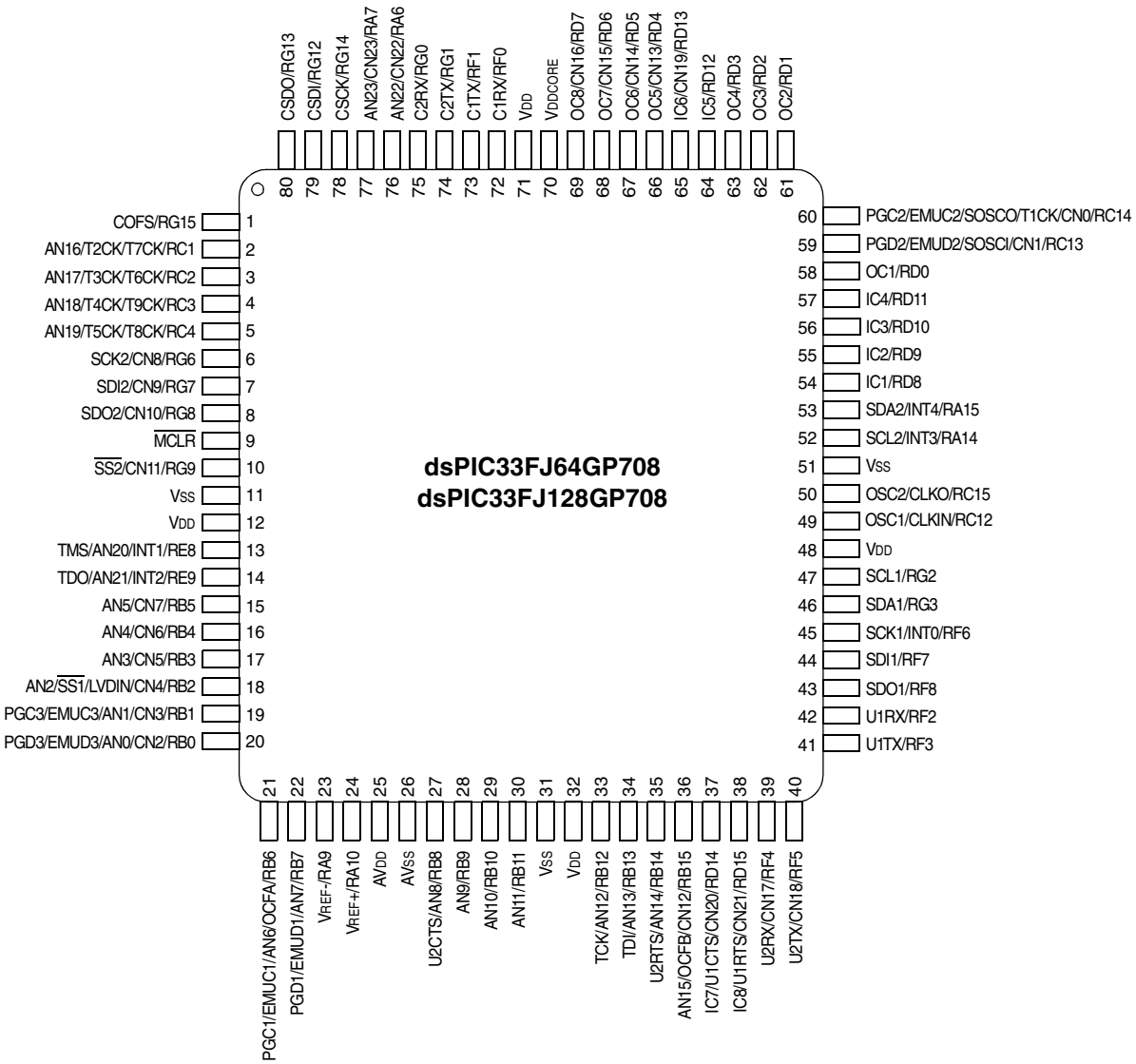
Pin Diagrams (Continued)

64-Pin TQFP



Pin Diagrams (Continued)

80-Pin TQFP



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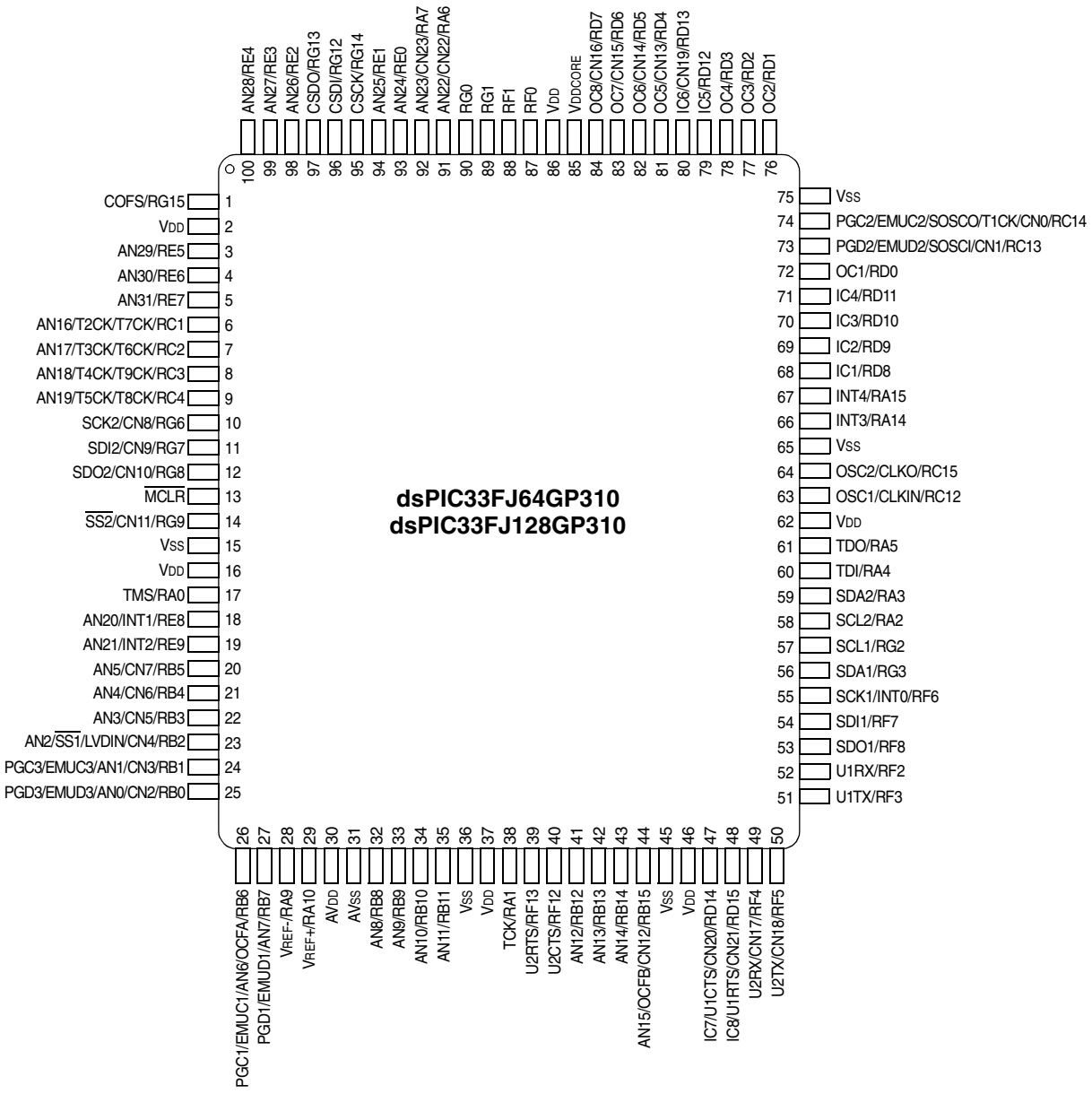
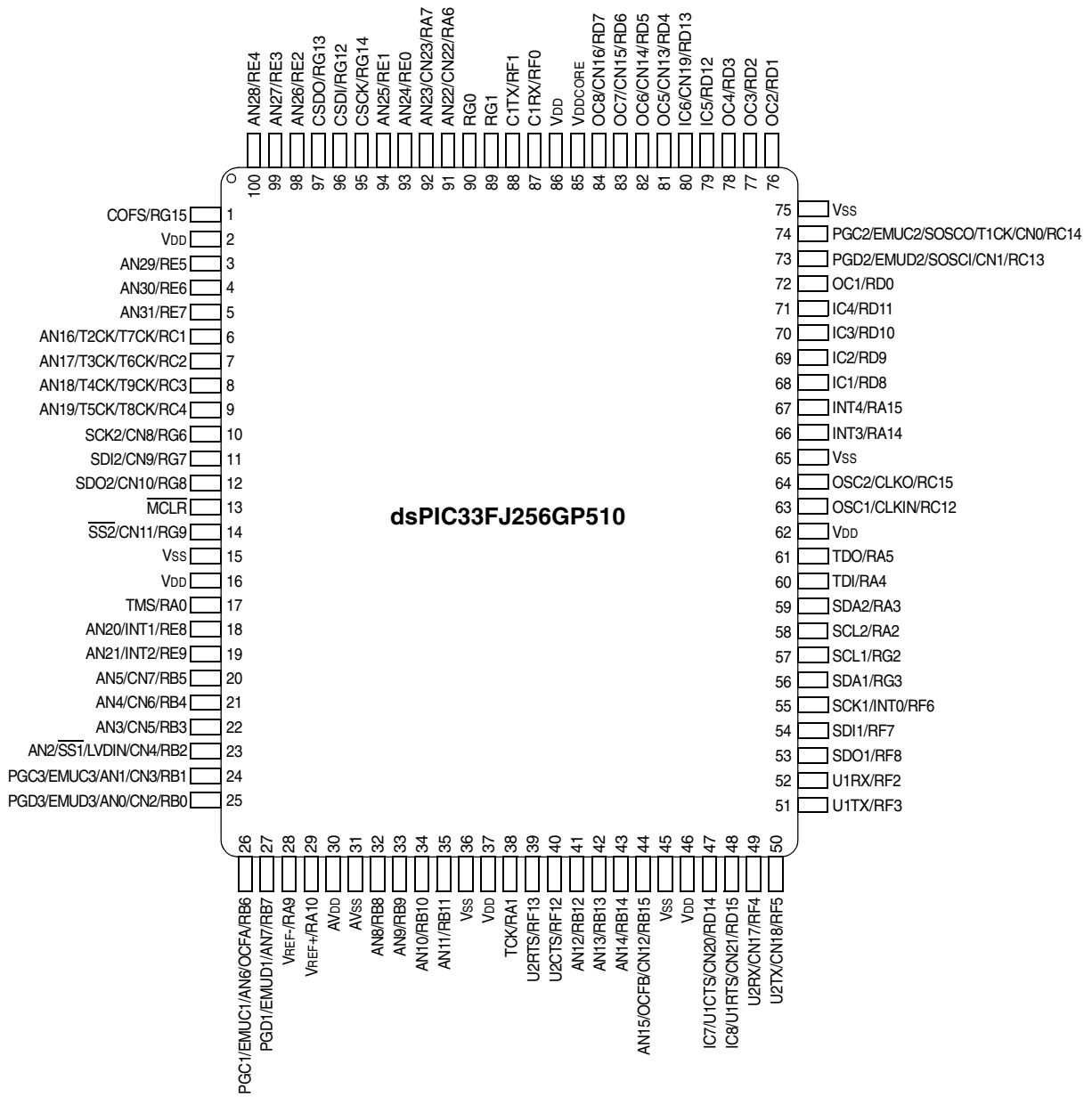
Pin Diagrams (Continued)

100-Pin TQFP



Pin Diagrams (Continued)

100-Pin TQFP



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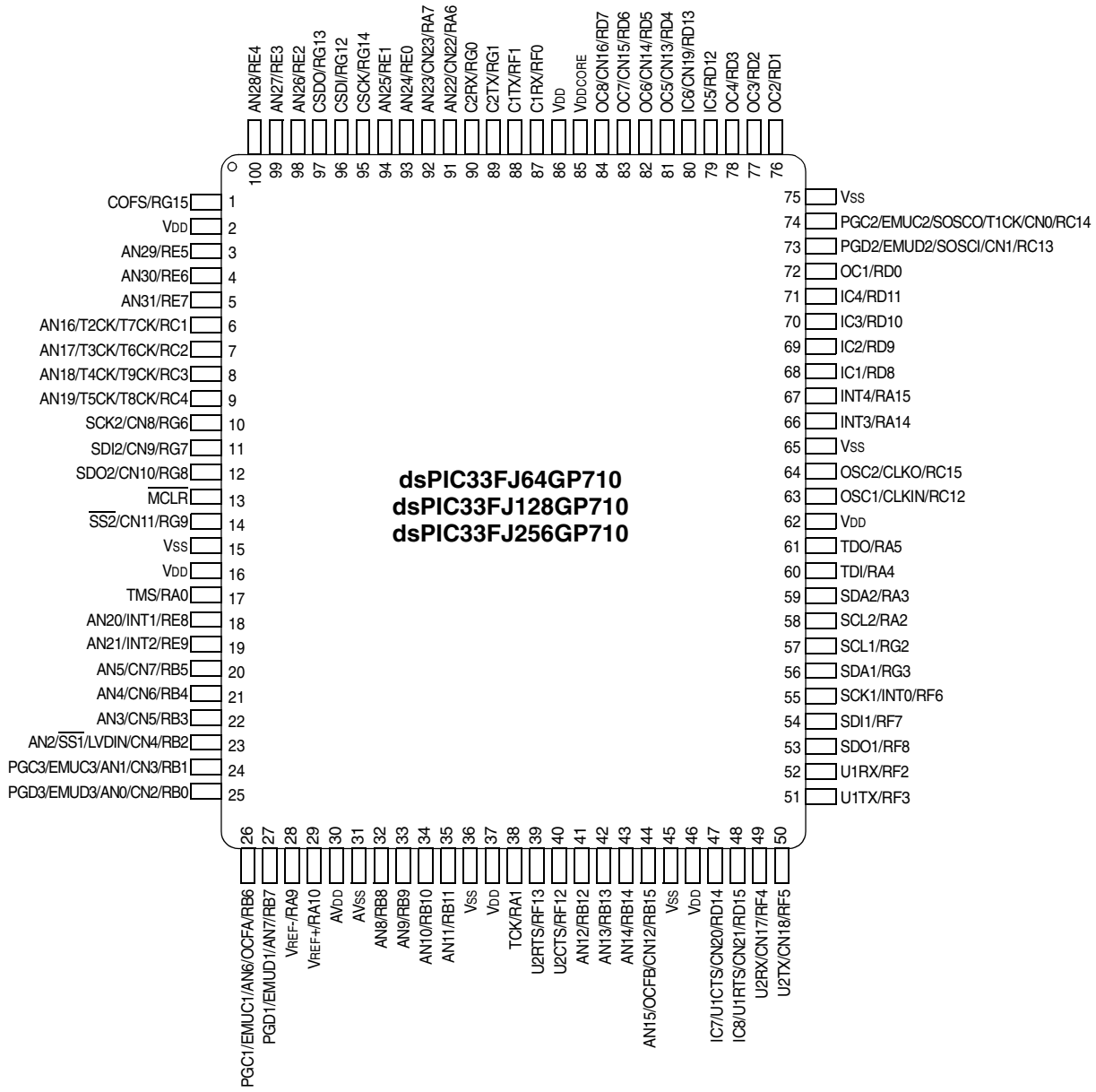
Pin Diagrams (Continued)

100-Pin TQFP



APPENDIX B: DEVICE I/O PINOUTS AND FUNCTIONS FOR MOTOR CONTROL FAMILY

Table B-1 provides a brief description of device I/O pinouts and the functions that may be multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE B-1: PINOUT I/O DESCRIPTIONS FOR MOTOR CONTROL FAMILY

Pin Name	Pin Type	Buffer Type	Description
AN0-AN23	I	Analog	Analog input channels. AN0 and AN1 are also used for device programming data and clock inputs, respectively.
AVDD	P	P	Positive supply for analog module.
AVSS	P	P	Ground reference for analog module.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
COFS CSCK CSDI CSDO	I/O I/O I O	ST ST ST —	Data Converter Interface frame synchronization pin. Data Converter Interface serial clock input/output pin. Data Converter Interface serial data input pin. Data Converter Interface serial data output pin.
C1RX C1TX C2RX C2TX	I O I O	ST — ST —	CAN1 bus receive pin. CAN1 bus transmit pin. CAN2 bus receive pin. CAN2 bus transmit pin.
PGD1/EMUD1 PGC1/EMUC1 PGD2/EMUD2 PGC2/EMUC2 PGD3/EMUD3 PGC3/EMUC3	I/O I I/O I I/O I	ST ST ST ST ST ST	Data I/O pin for programming/debugging communication channel 1. Clock input pin for programming/debugging communication channel 1. Data I/O pin for programming/debugging communication channel 2. Clock input pin for programming/debugging communication channel 2. Data I/O pin for programming/debugging communication channel 3. Clock input pin for programming/debugging communication channel 3.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INDX QEA QEB UPDN	I I I O	ST ST ST CMOS	Quadrature Encoder Index Pulse input. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Position Up/Down Counter Direction State.
INT0 INT1 INT2 INT3 INT4	I I I I I	ST ST ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2. External interrupt 3. External interrupt 4.
FLTA FLTB PWM1L PWM1H PWM2L PWM2H PWM3L PWM3H PWM4L PWM4H	I I O O O O O O O O	ST ST — — — — — — — —	PWM Fault A input. PWM Fault B input. PWM 1 low output. PWM 1 high output. PWM 2 low output. PWM 2 high output. PWM 3 low output. PWM 3 high output. PWM 4 low output. PWM 4 high output.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; P = Power

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TABLE B-1: PINOUT I/O DESCRIPTIONS FOR MOTOR CONTROL FAMILY (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
MCLR	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active-low Reset to the device.
OCFA OCFB OC1-OC8	I I O	ST ST —	Compare Fault A input (for Compare Channels 1, 2, 3 and 4). Compare Fault B input (for Compare Channels 5, 6, 7 and 8). Compare outputs 1 through 8.
OSC1 OSC2	I I/O	ST/CMOS —	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
RA0-RA7 RA9-RA10 RA12-RA15	I/O I/O I/O	ST ST ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1-RC4 RC12-RC15	I/O I/O	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8 RF12-RF13	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG3 RG6-RG9 RG12-RG15	I/O I/O I/O	ST ST ST	PORTG is a bidirectional I/O port.
SCK1 SDI1 SDO1 SS1 SCK2 SDI2 SDO2 SS2	I/O I O I I/O I O I	ST ST — ST ST ST — ST	Synchronous serial clock input/output for SPI1. SPI1 data in. SPI1 data out. SPI1 slave synchronization. Synchronous serial clock input/output for SPI2. SPI2 data in. SPI2 data out. SPI2 slave synchronization.
SCL1 SDA1 SCL2 SDA2	I/O I/O I/O I/O	ST ST ST ST	Synchronous serial clock input/output for I2C1. Synchronous serial data input/output for I2C1. Synchronous serial clock input/output for I2C2. Synchronous serial data input/output for I2C2.
SOSCI SOSCO	I O	ST/CMOS —	32 kHz low-power oscillator crystal input; CMOS otherwise. 32 kHz low-power oscillator crystal output.
TMS TCK TDI TDO	I I/O I O	ST ST ST —	JTAG Test mode select pin. JTAG test clock input/output pin. JTAG test data input pin. JTAG test data output pin.
T1CK T2CK T3CK T4CK T5CK T6CK T7CK T8CK T9CK	I I I I I I I I I	ST ST ST ST ST ST ST ST ST	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input. Timer6 external clock input. Timer7 external clock input. Timer8 external clock input. Timer9 external clock input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; P = Power

TABLE B-1: PINOUT I/O DESCRIPTIONS FOR MOTOR CONTROL FAMILY (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
U1CTS	I	ST	UART1 clear to send.
U1RTS	O	—	UART1 ready to send.
U1RX	I	ST	UART1 receive.
U1TX	O	—	UART1 transmit.
U2CTS	I	ST	UART2 clear to send.
U2RTS	O	—	UART2 ready to send.
U2RX	I	ST	UART2 receive.
U2TX	O	—	UART2 transmit.
VDD	P	—	Positive supply for peripheral logic and I/O pins.
VDDCORE	P	—	CPU logic filter capacitor connection.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog voltage reference (high) input.
VREF-	I	Analog	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; P = Power

TABLE B-2: dsPIC33F MOTOR CONTROL FAMILY VARIANTS (DEVICES MARKED "PS")

Device	Pins	Program Flash Memory (KB)	RAM (KB)(1)	Timer 16-bit	Input Capture	Output Compare Std. PWM	Motor Control PWM	Quadrature Encoder Interface	Codec Interface	A/D Converter	UART	SPI™	I²C™	CAN	I/O Pins (Max)(2)	Packages
33FJ128MC706	64	128	17	9	8	8	8 ch	1	0	2 A/D, 16 ch	2	2	2	1	53	PT
33FJ128MC708	80	128	17	9	8	8	8 ch	1	0	2 A/D, 18 ch	2	2	2	1	69	PT
33FJ256MC710	100	256	33	9	8	8	8 ch	1	0	2 A/D, 24 ch	2	2	2	2	86	PF

Note 1: RAM size is inclusive of 1 KB DMA RAM.
2: Maximum I/O pin count includes pins shared by the peripheral functions.

Note: Prototype samples are intended for dsPIC33F early adopters and are based on early revision silicon. Devices are marked with "PS" suffix. Major differences are noted in this data sheet. For additional information, please refer to the *"ds*PIC33F *Data Sheet"*.

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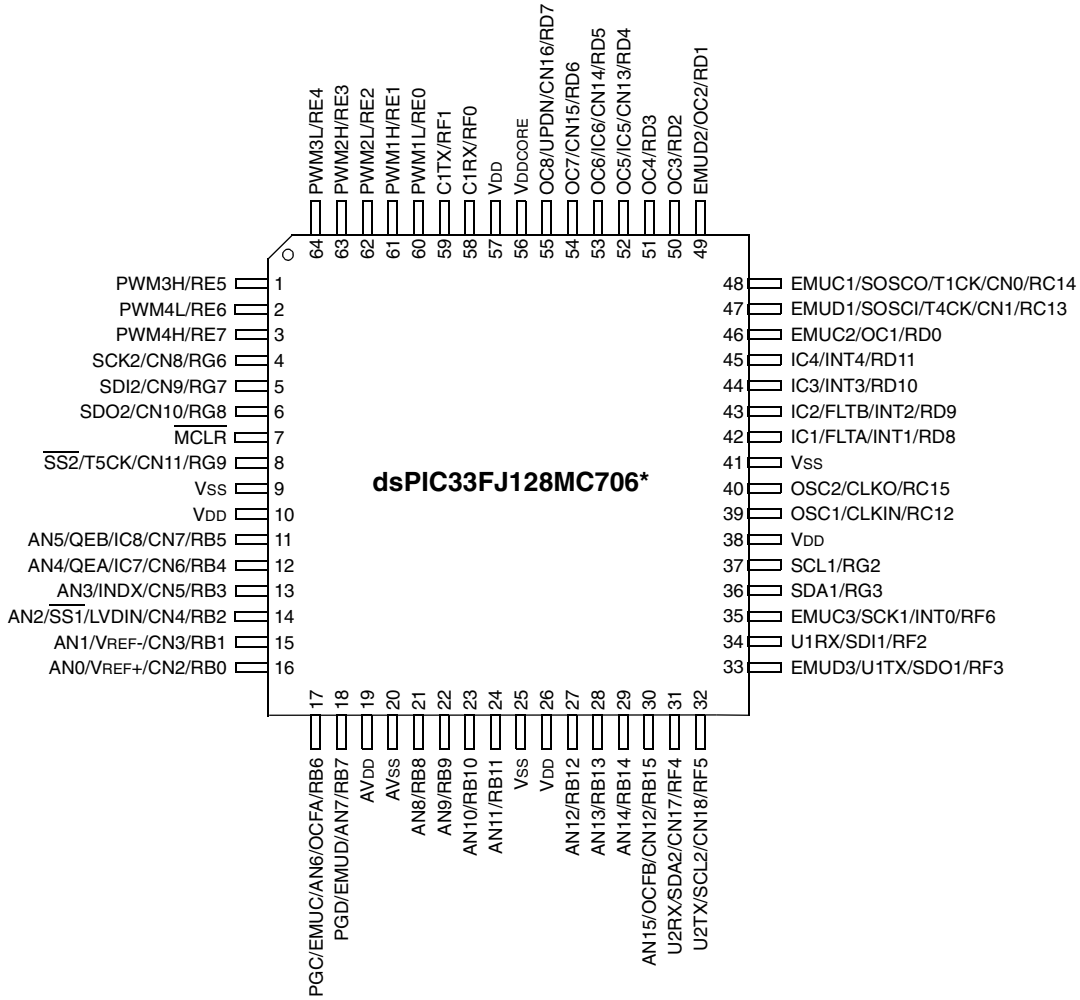
Pin Diagrams

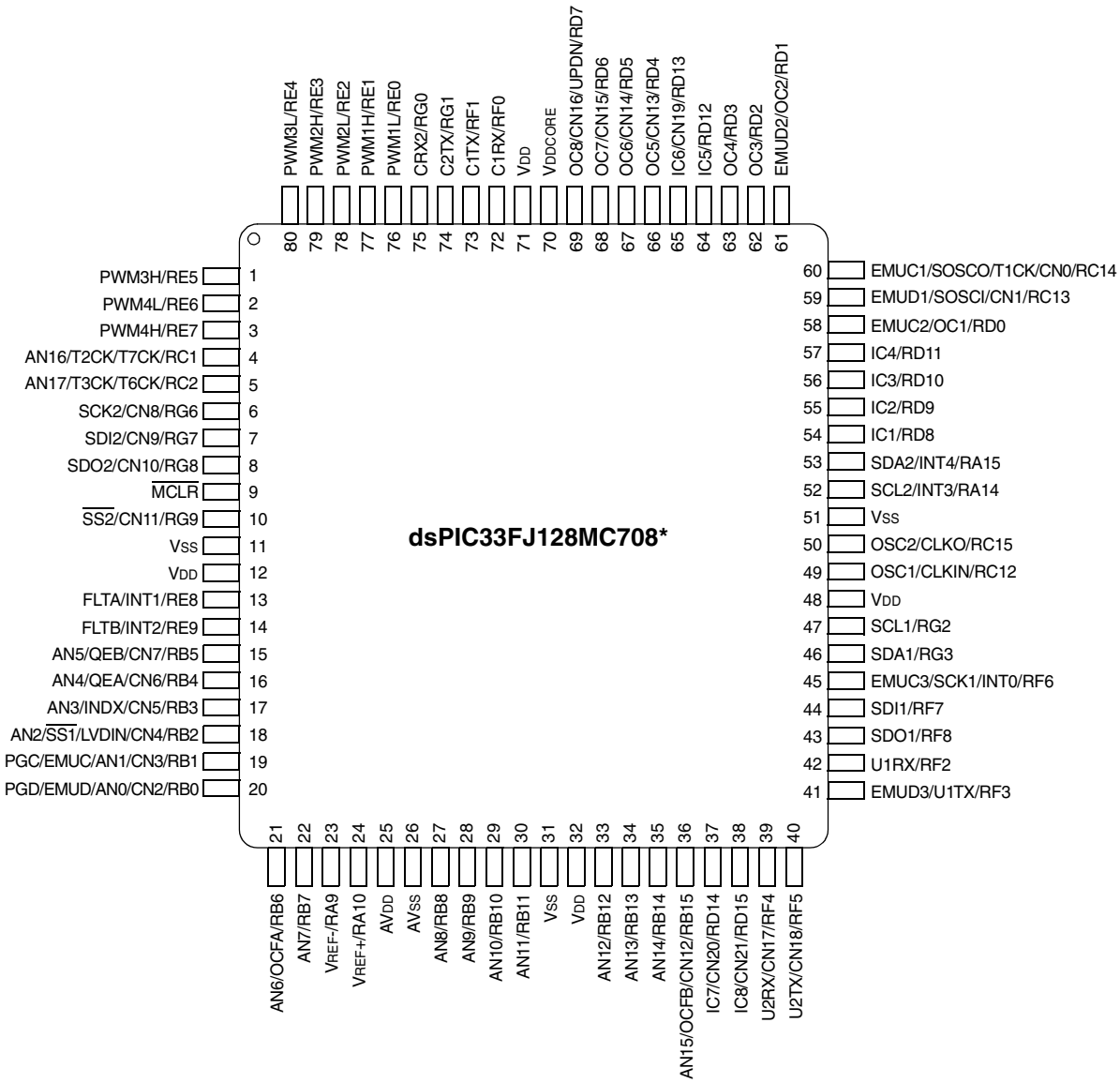
64-Pin TQFP



*Device is marked with ‘PS’ designator.

Pin Diagrams (Continued)

80-Pin TQFP



*Device is marked with ‘PS’ designator.

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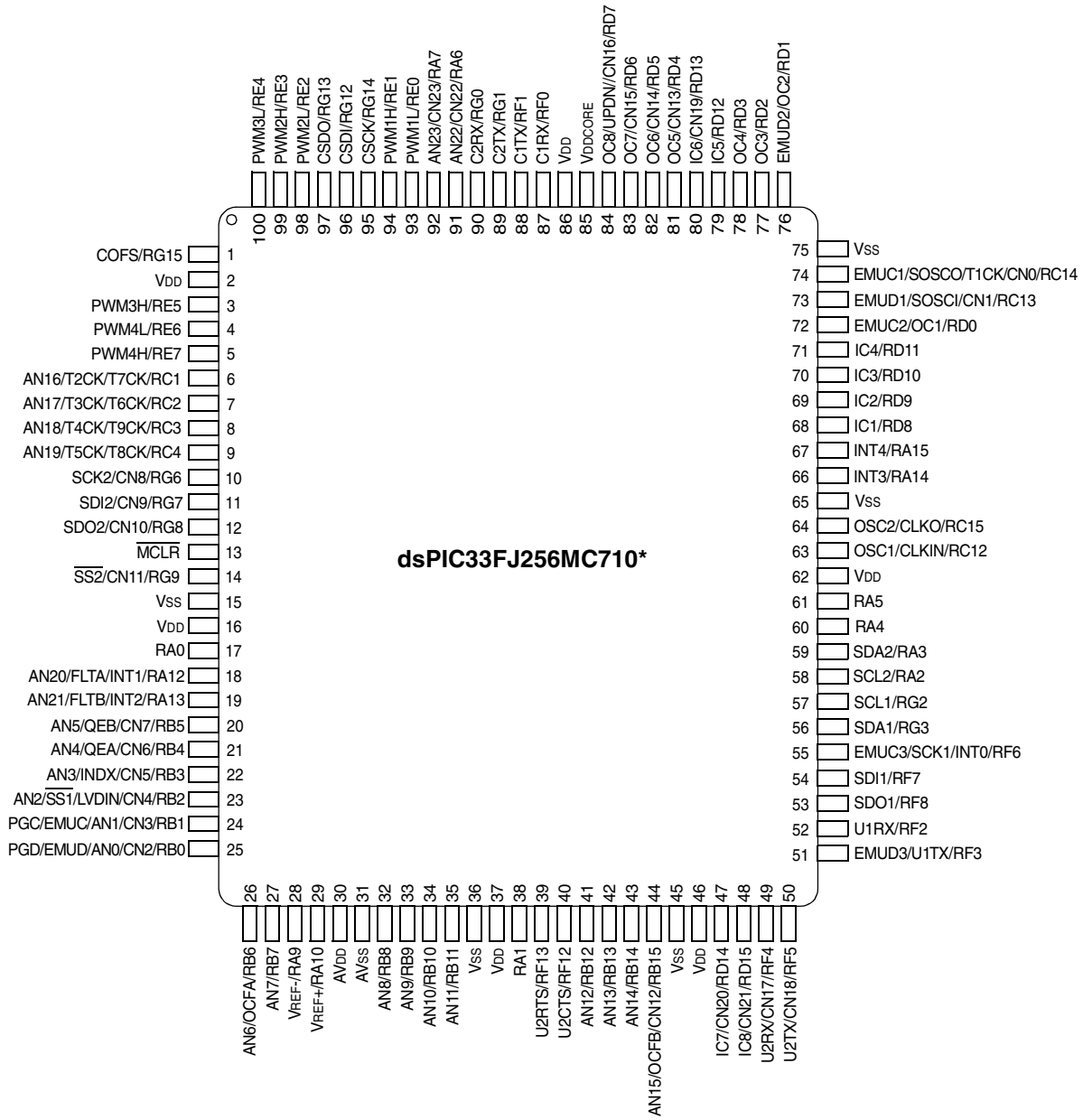
Pin Diagrams (Continued)

100-Pin TQFP



*Device is marked with 'PS' designator.

Pin Diagrams (Continued)

64-Pin TQFP

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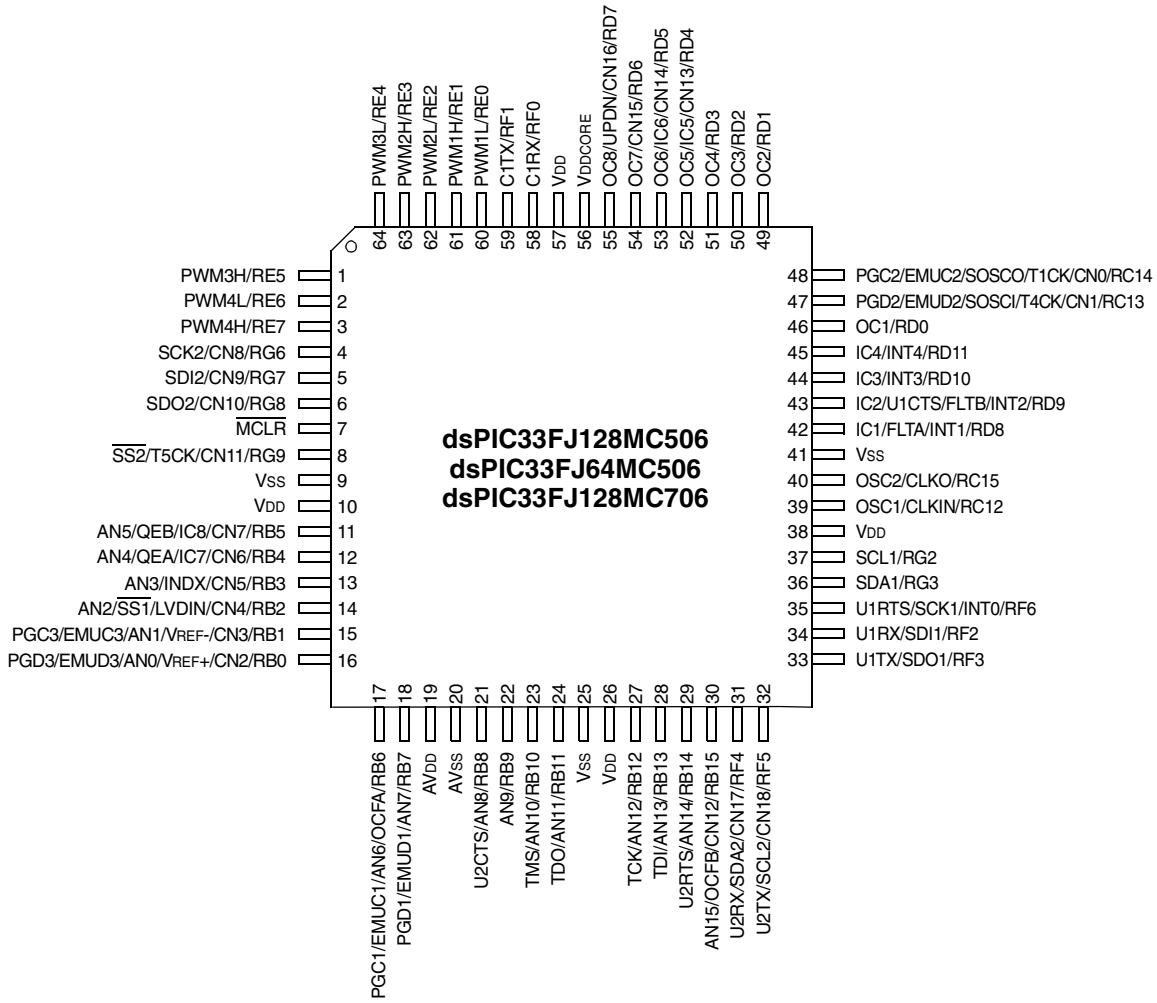
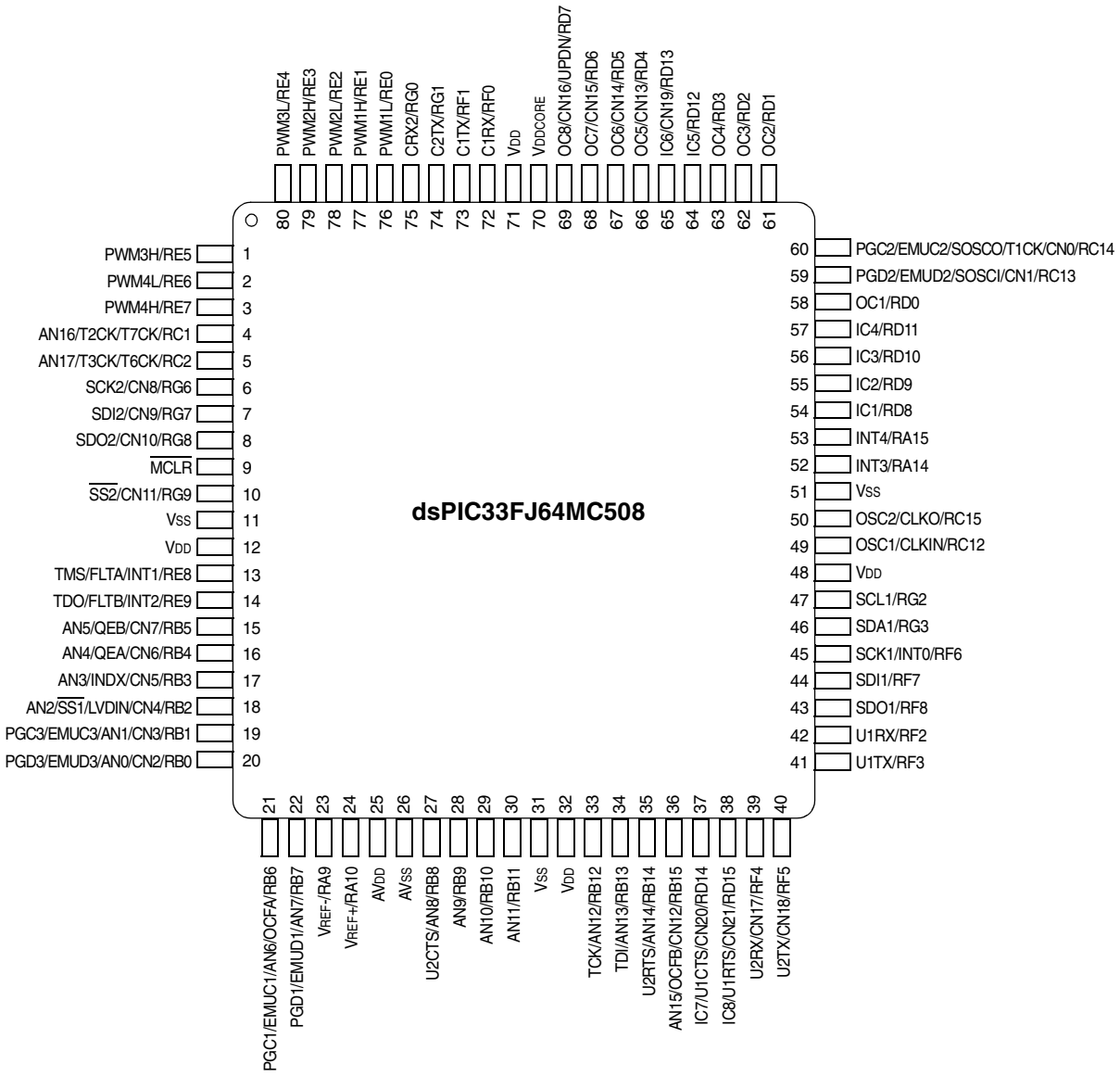
Pin Diagrams (Continued)

64-Pin TQFP



Pin Diagrams (Continued)

80-Pin TQFP



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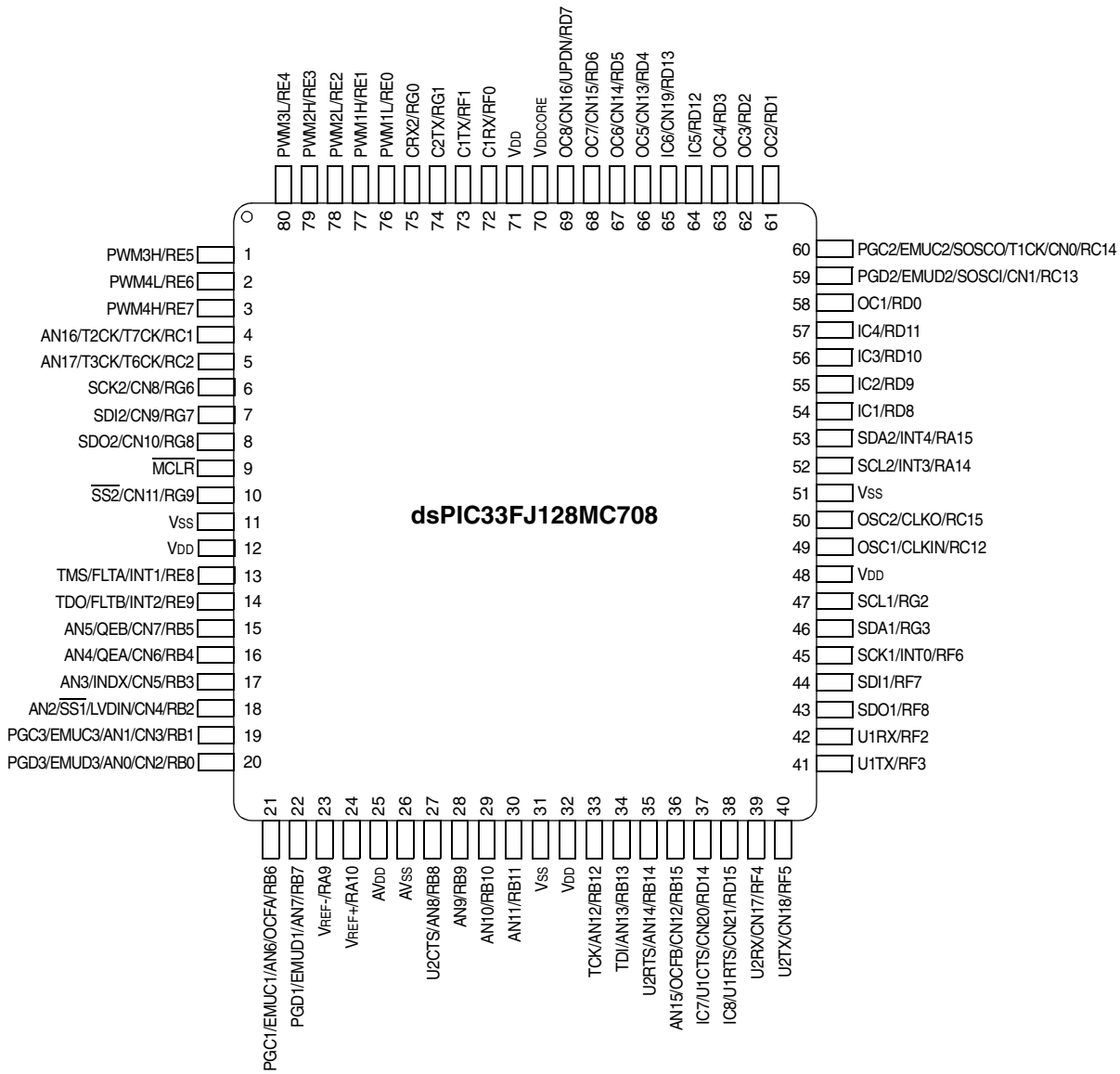
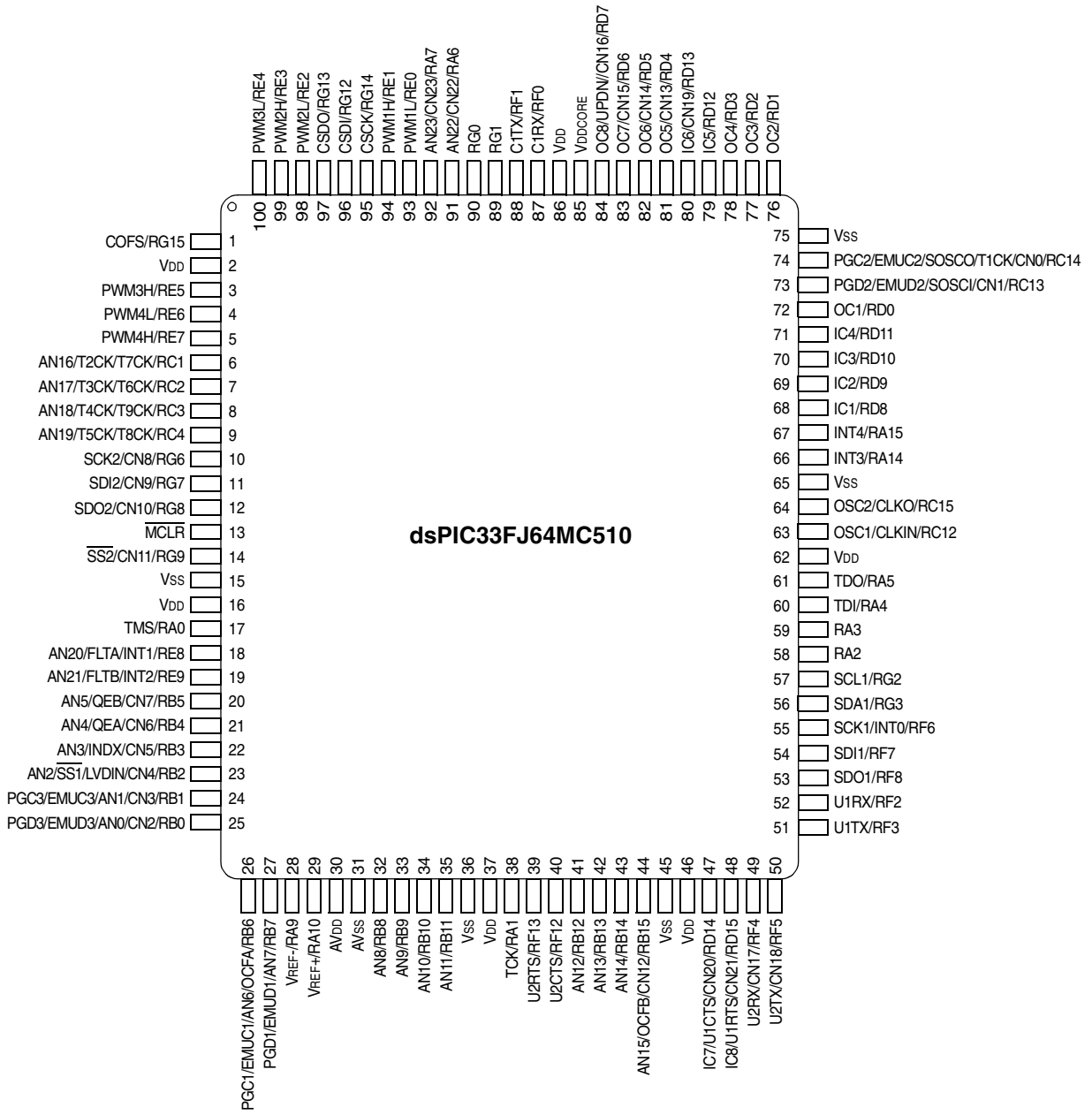
Pin Diagrams (Continued)

80-Pin TQFP



Pin Diagrams (Continued)

100-Pin TQFP



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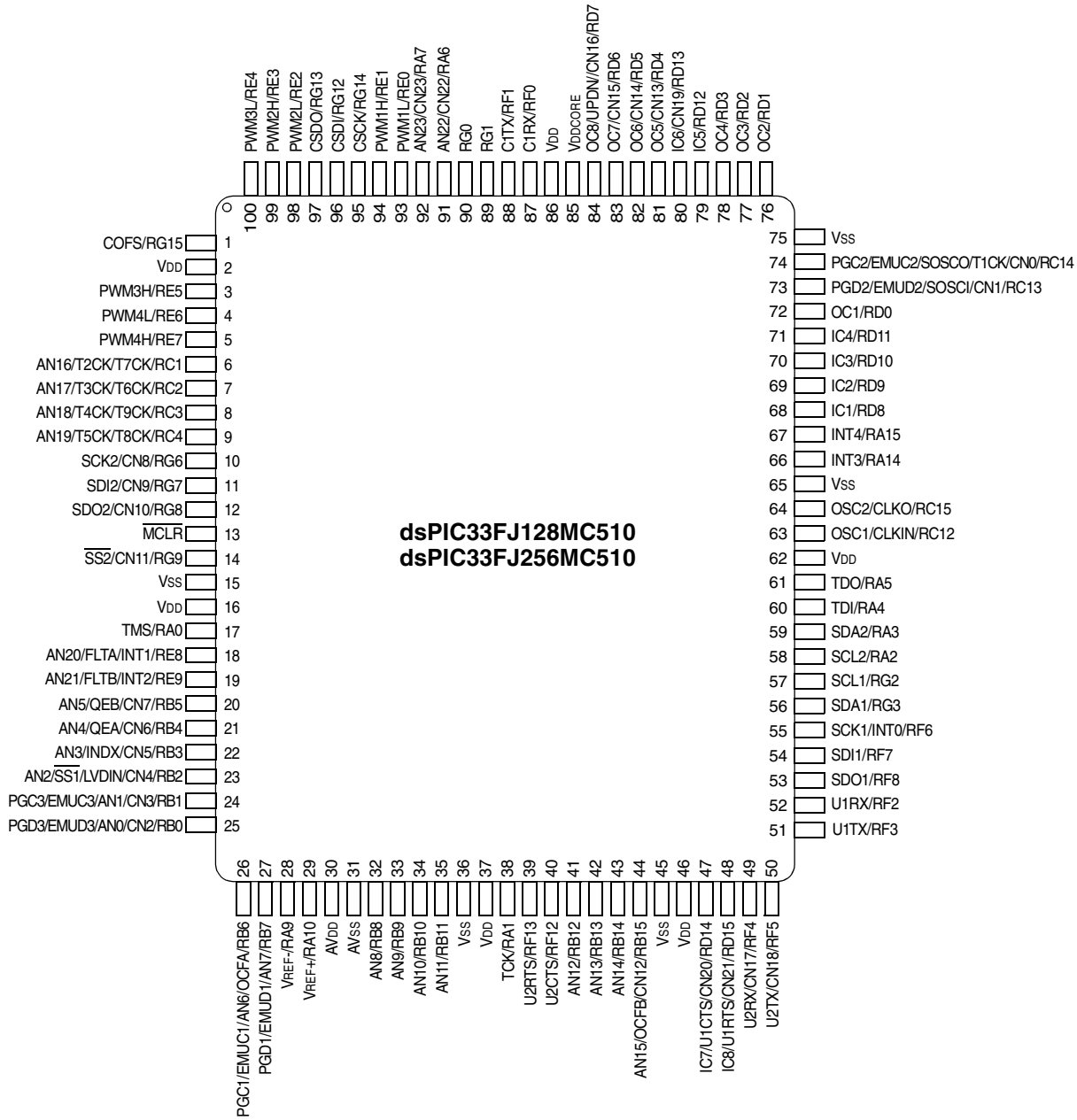
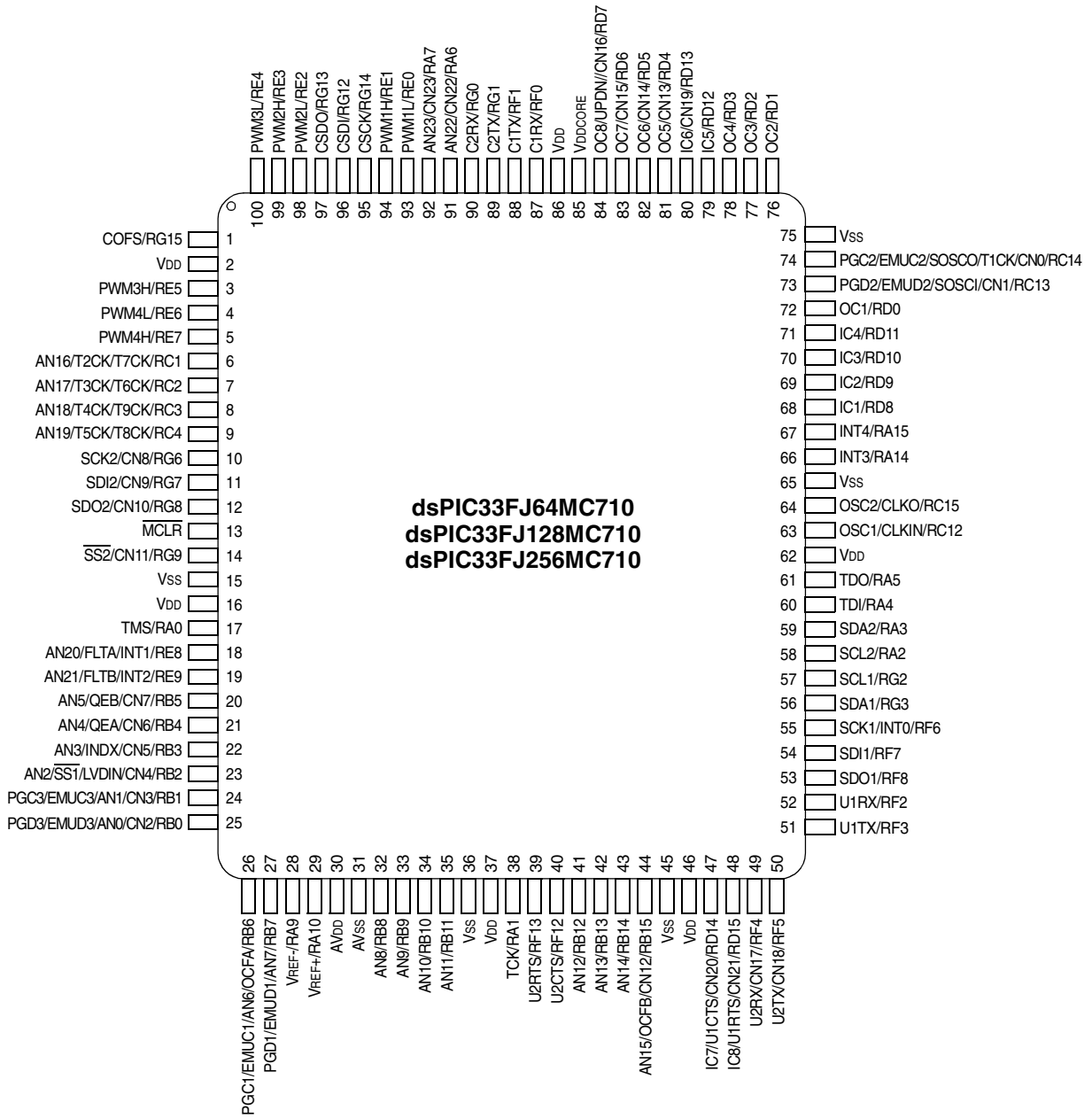
Pin Diagrams (Continued)

100-Pin TQFP



Pin Diagrams (Continued)

100-Pin TQFP



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