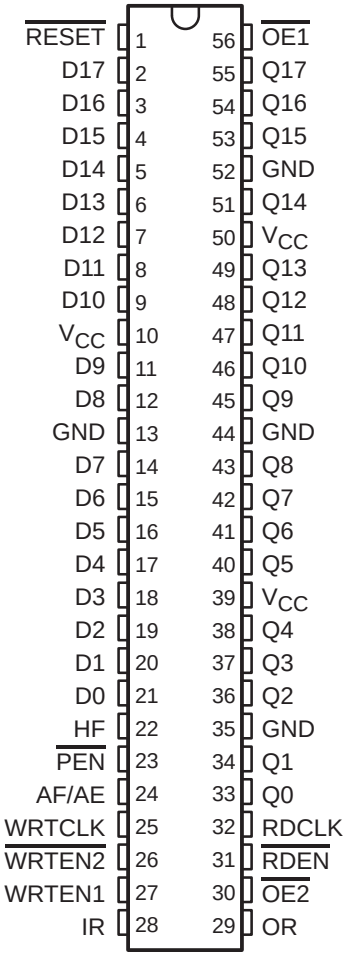
- **Member of the Texas Instruments Widebus™ Family**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates up to 67 MHz**
- **Pin-to-Pin Compatible With SN74ACT7803 and SN74ACT7805**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

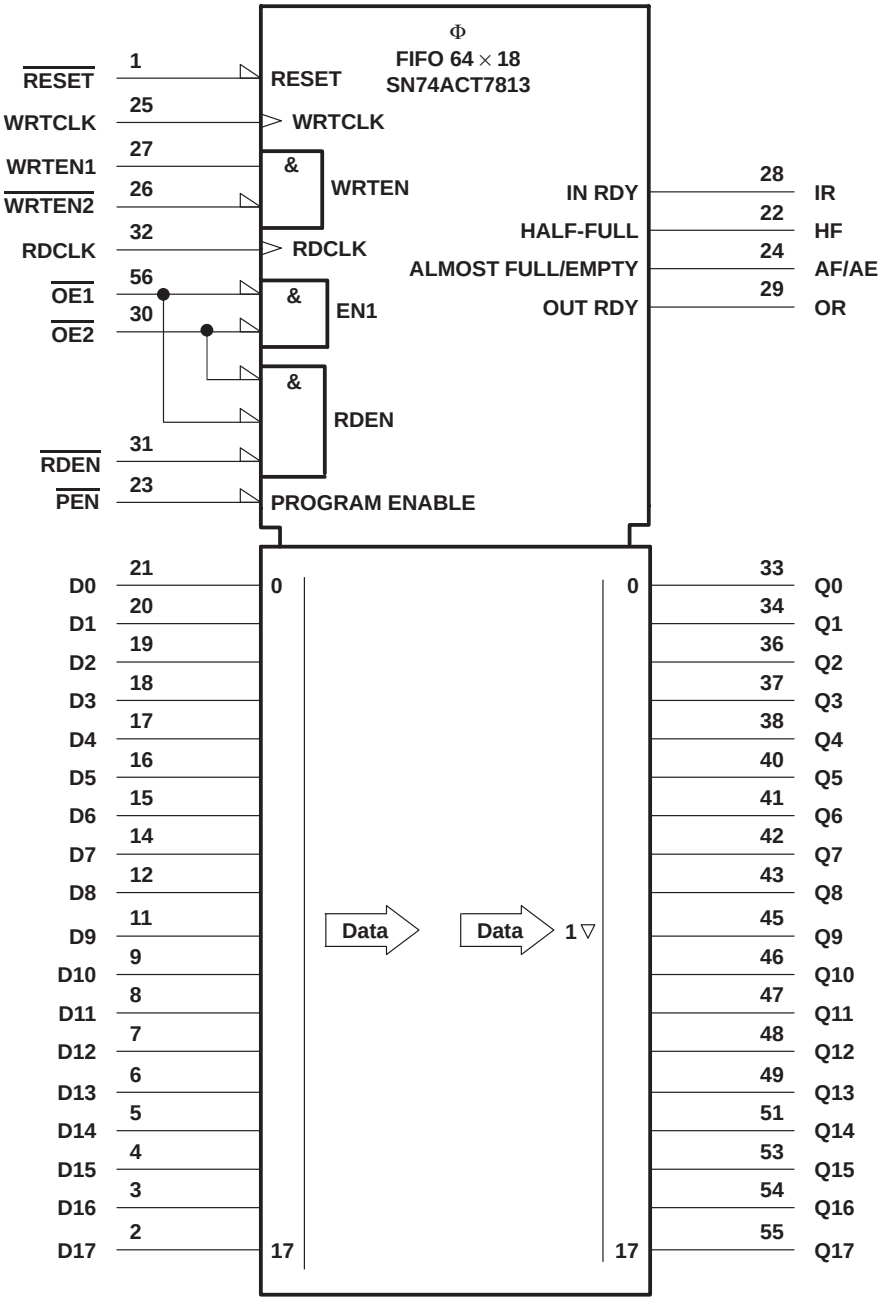
The SN74ACT7813 is a 64-word × 18-bit FIFO suited for buffering asynchronous datapaths up to 67-MHz clock rates and 12-ns access times. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins, along with Texas Instruments patented output edge control (OEC™) circuit, dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) are free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and input ready (IR) is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and output ready (OR) is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and half-full (HF) flags low and the almost-full/almost-empty (AF/AE) flag high. The FIFO must be reset upon power up.

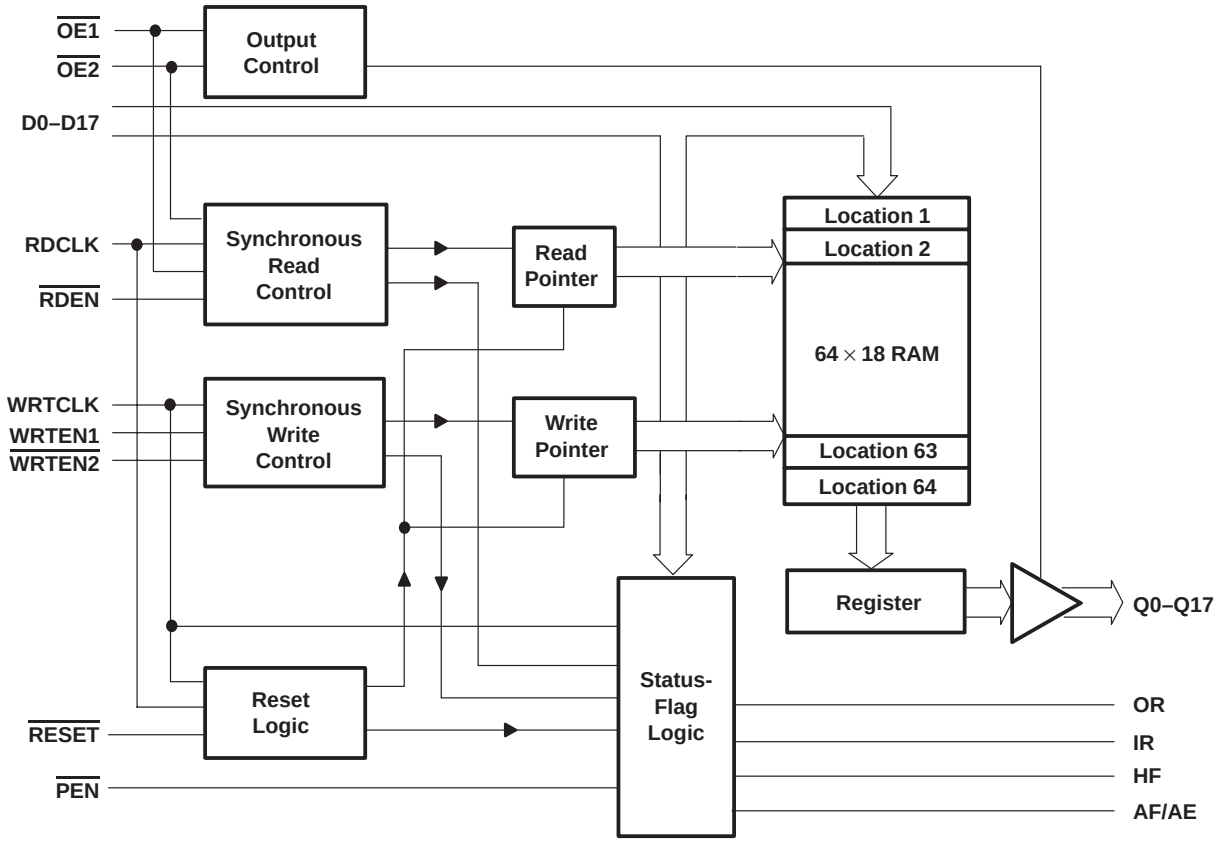
The SN74ACT7813 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 8 can be used for both the AE offset (X) and the AF offset (Y). AF/AE is high when memory contains X or fewer words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{OE1}$, $\overline{OE2}$	56, 30	I	Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{PEN}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	The 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR also is asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
$\overline{RDEN}$	31	I	Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{RESET}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{WRTEN2}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

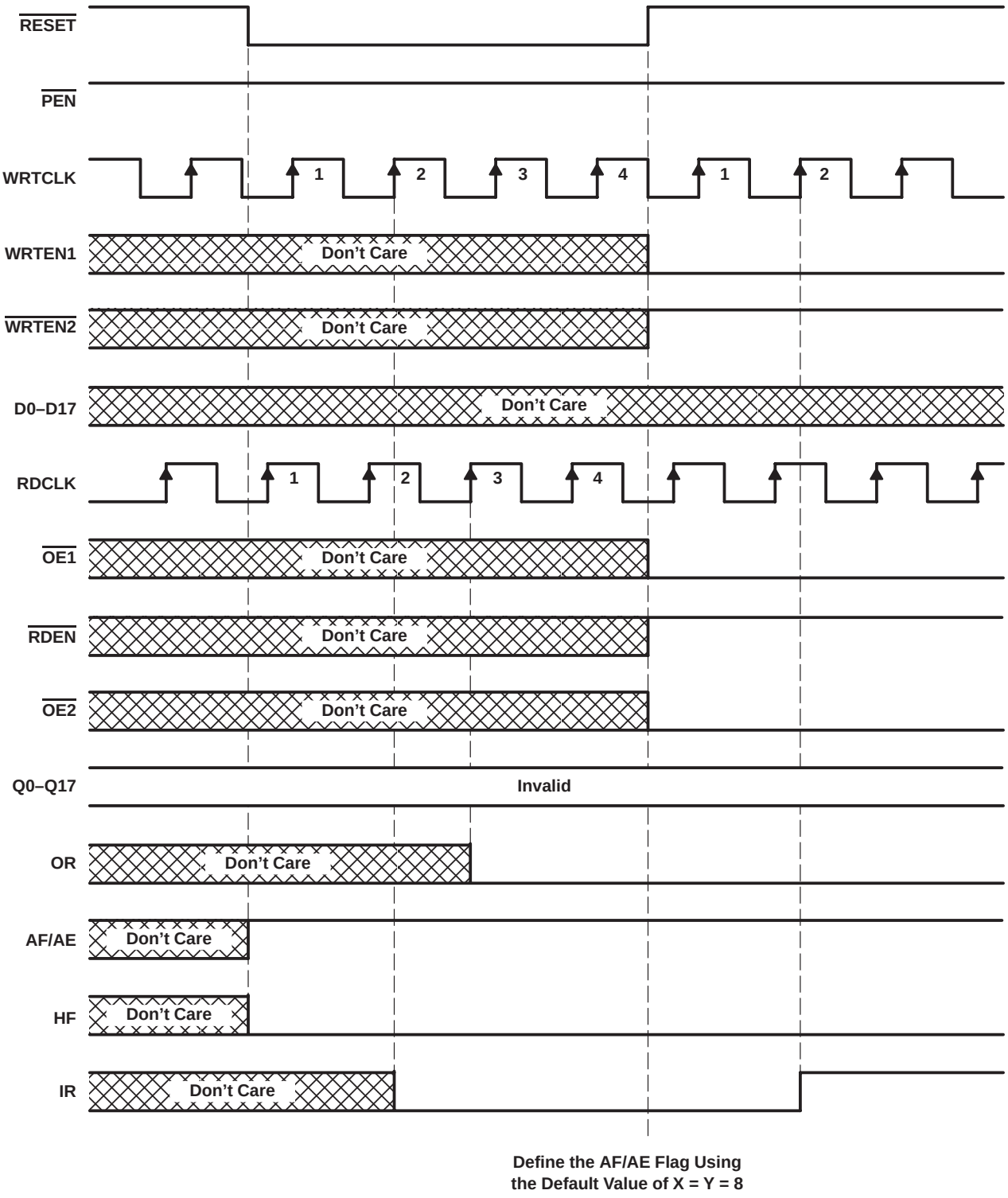


Figure 1. Reset Cycle

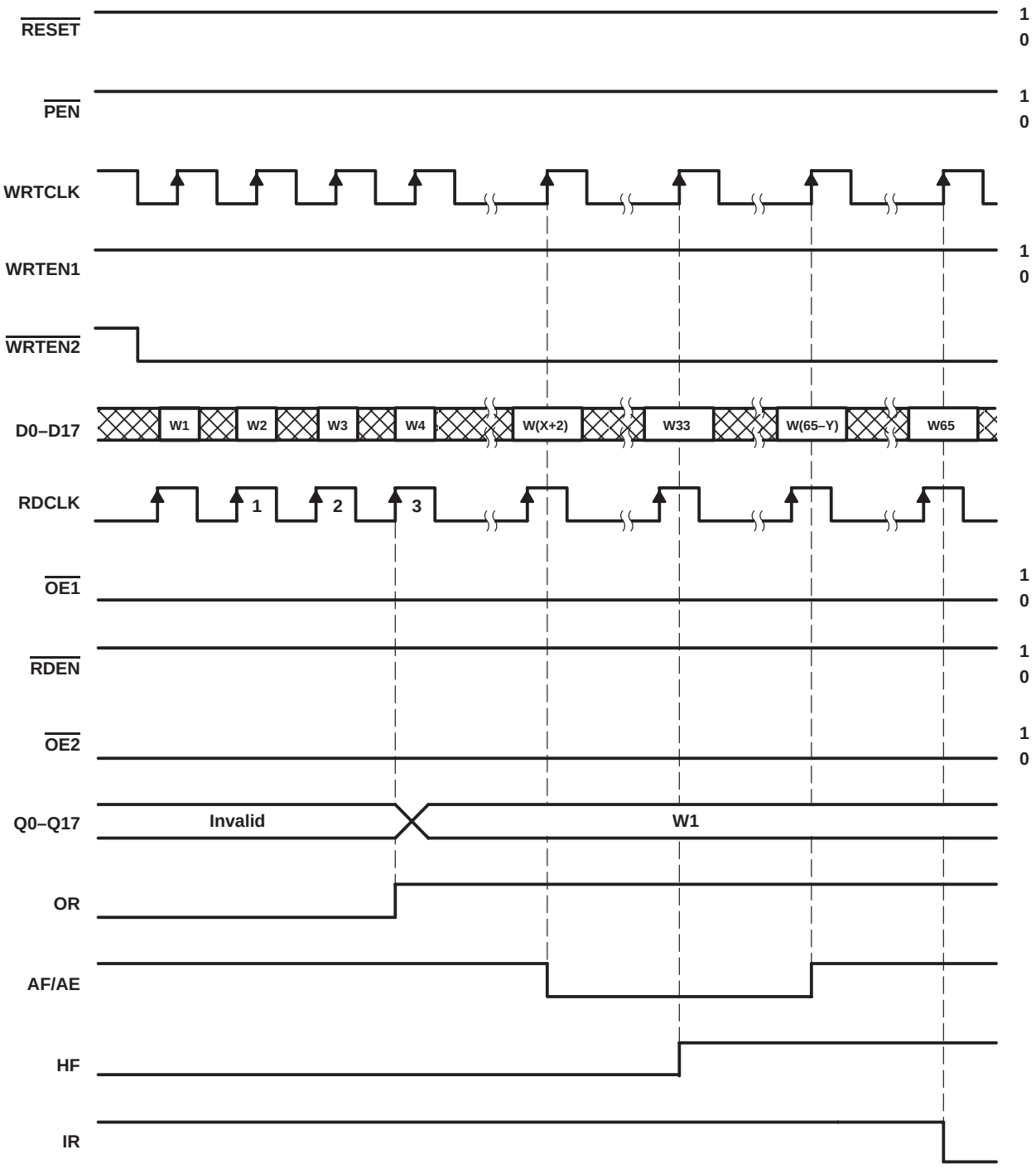


Figure 2. Write Cycle

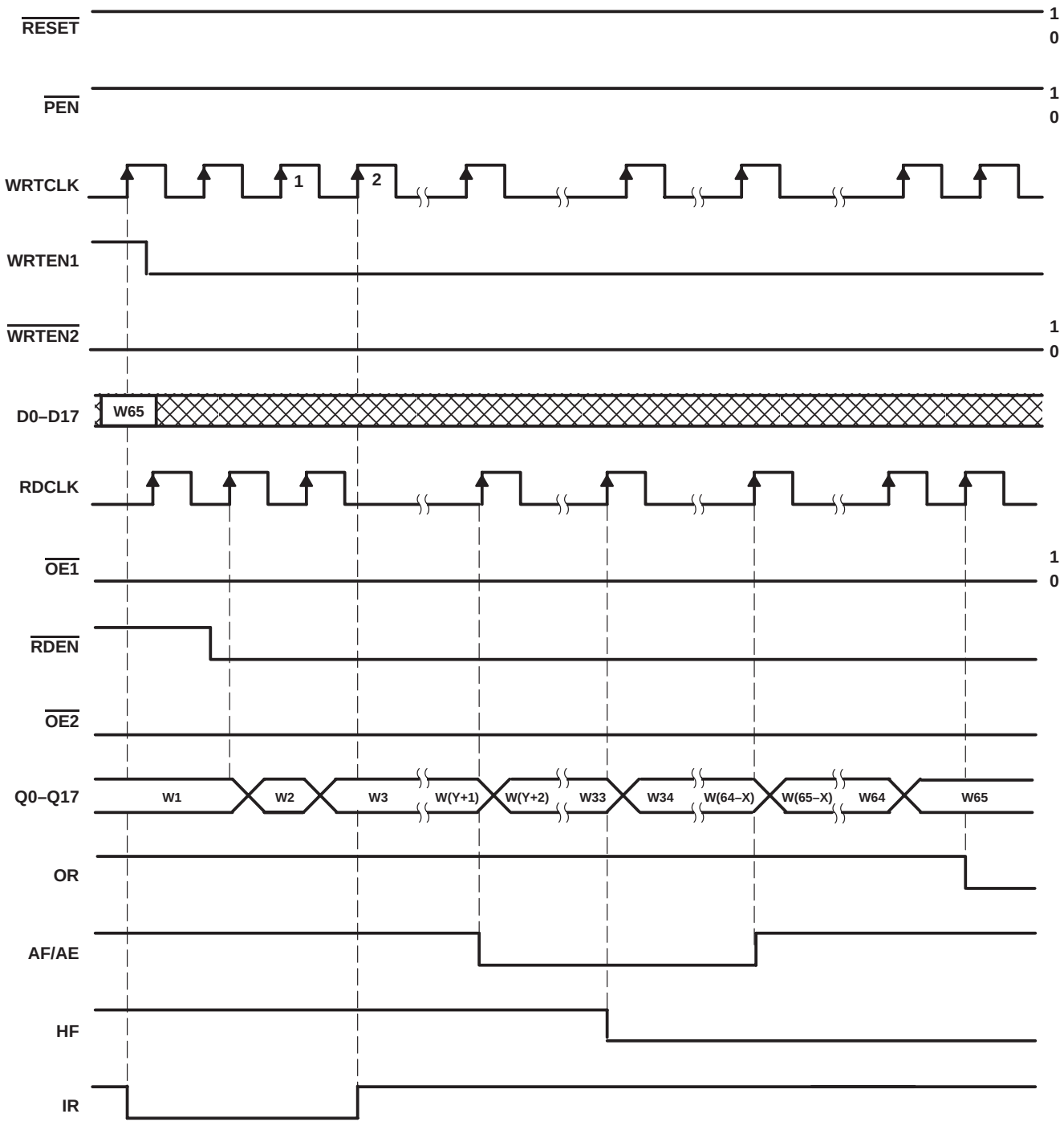


Figure 3. Read Cycle

offset values for AF/AE

The AF/AE flag has two programmable limits: the AE offset value (X) and the AF offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 8 are used. The AF/AE flag is high when the FIFO contains X or fewer words or (64 – Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D4 is stored as the AE offset value (X) and the AF offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D4 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 31 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 8, $\overline{PEN}$ must be held high.

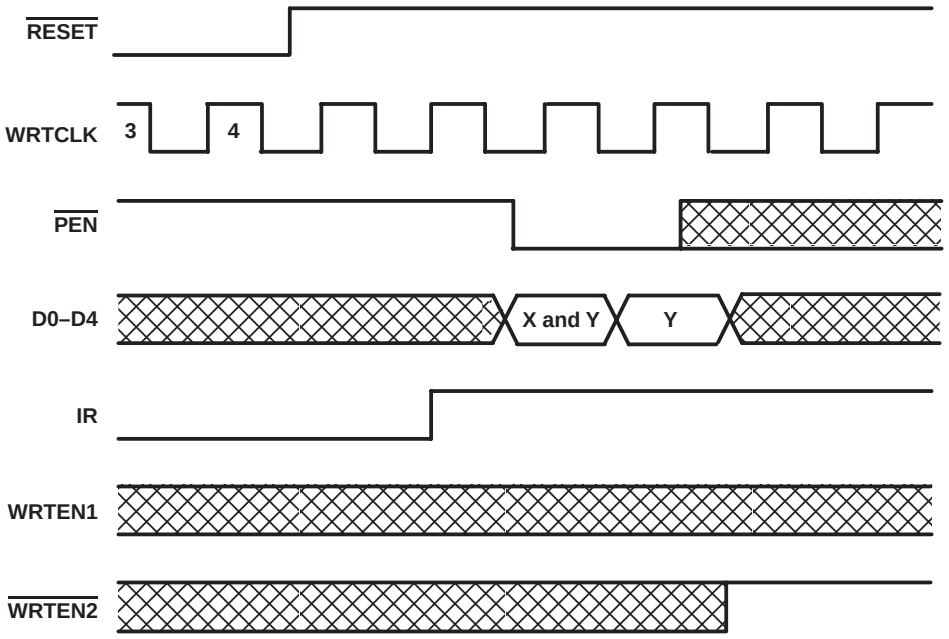


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 74°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			’ACT7813-15		’ACT7813-20		’ACT7813-25		’ACT7813-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, flags		–8		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 5)

			’ACT7813-15		’ACT7813-20		’ACT7813-25		’ACT7813-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{PEN}$ low	8		9		9		12		
t_{su}	Setup time	D0–D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑	4		5		5		5		
		$\overline{OE1}$, $\overline{OE2}$ before RDCLK↑	5		5		6		6		
		$\overline{RDEN}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		6		6		
		$\overline{PEN}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑	0		0		0		0		
		$\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	2		2		2		2		
		$\overline{PEN}$ high after WRTCLK↓	0		0		0		0		
		$\overline{PEN}$ low after WRTCLK↑	2		2		2		2		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figure 5)

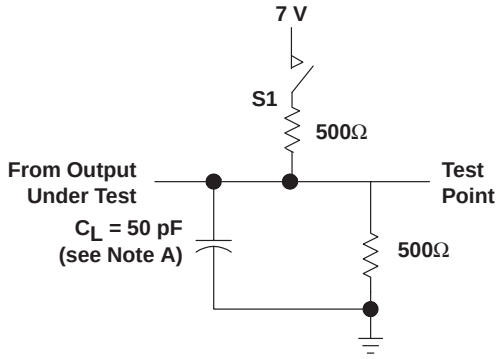
PARAMETER	FROM (INPUT)	TO (OUTPUT)	’ACT7813-15			’ACT7813-20		’ACT7813-25		’ACT7813-40		UNIT
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§	RDCLK↑	Any Q		8.5								ns
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	
	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	
	RDCLK↑		7		17	7	19	7	21	7	23	
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑	HF	7		15.5	7	18	7	20	7	22	ns
t_{PLH}	$\overline{RESET}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}	$\overline{RESET}$ low	HF	2		10	2	12	2	14	2	16	ns
t_{en}	$\overline{OE1}$, $\overline{OE2}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}	$\overline{OE1}$, $\overline{OE2}$	Any Q	2		9.5	2	11	2	14	2	14	ns

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This parameter is measured with a 30-pF load (see Figure 6).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

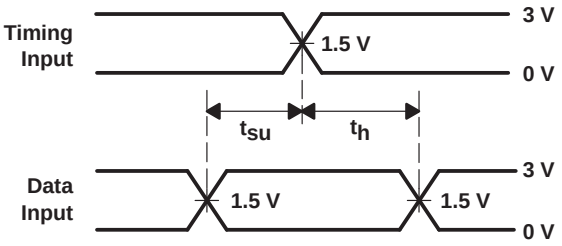
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

PARAMETER MEASUREMENT INFORMATION

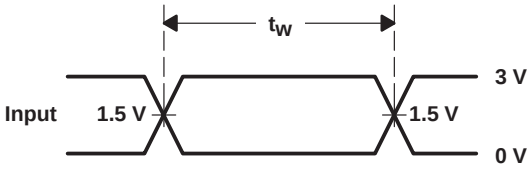


LOAD CIRCUIT

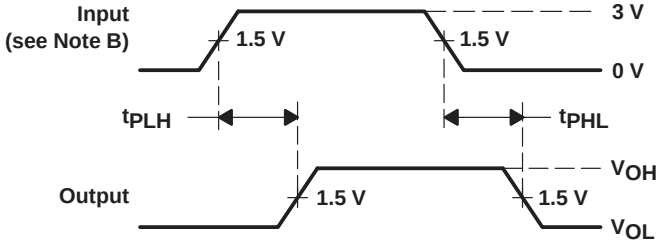
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



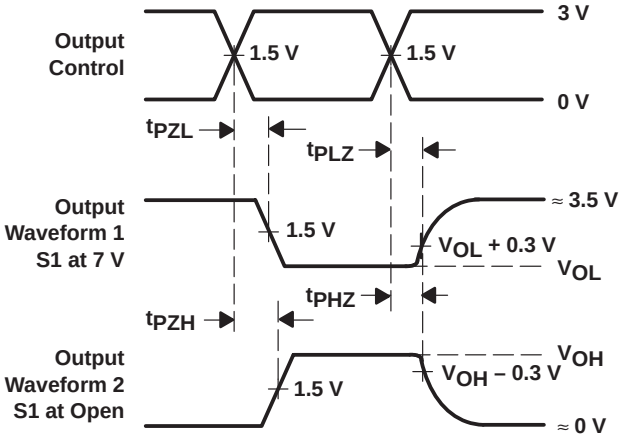
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

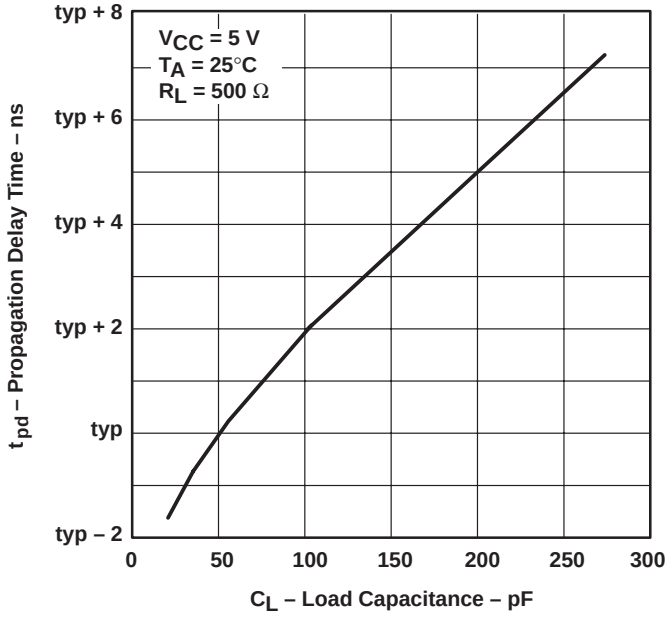


Figure 6

SUPPLY CURRENT vs CLOCK FREQUENCY

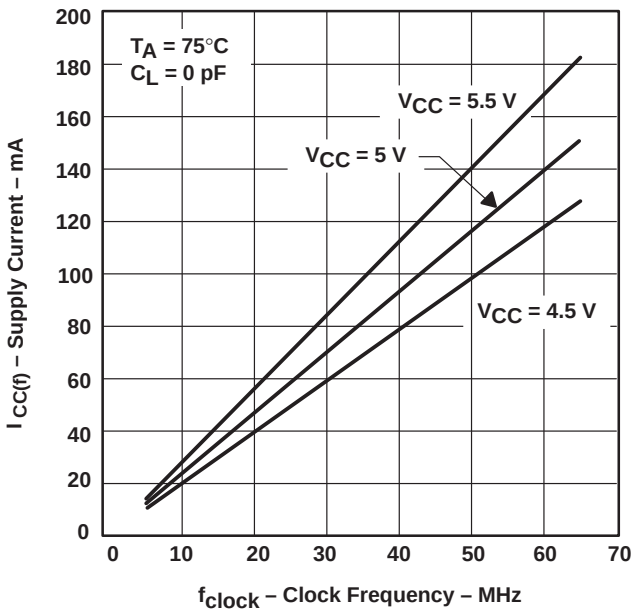


Figure 7

APPLICATION INFORMATION

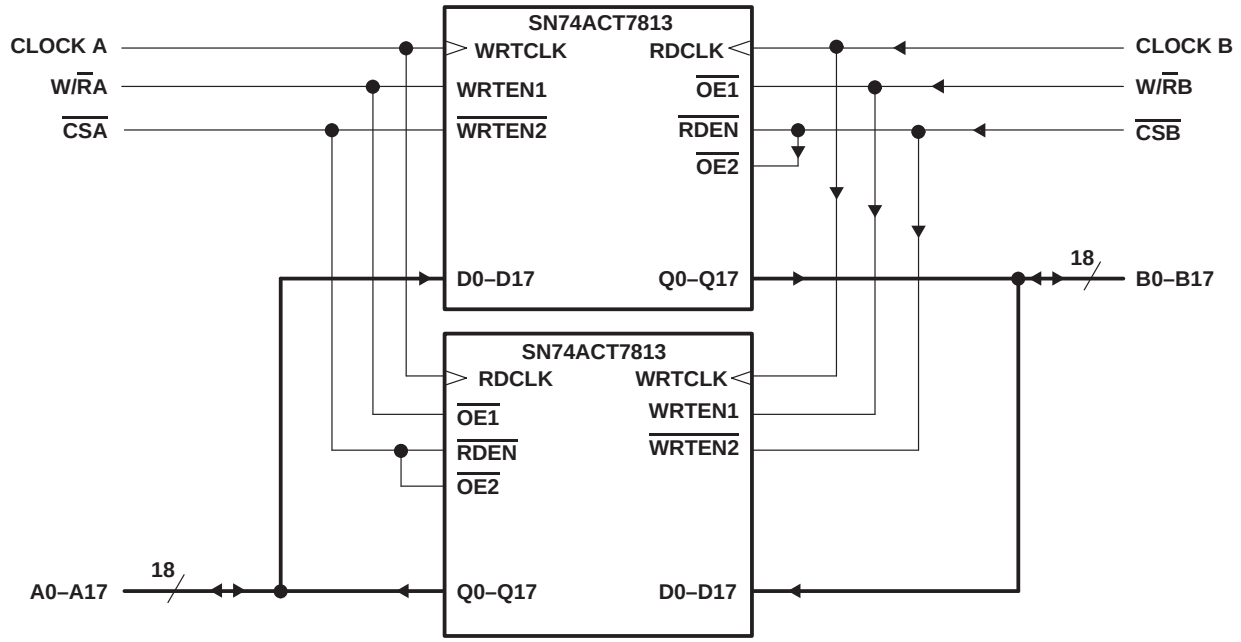


Figure 8. Bidirectional Configuration

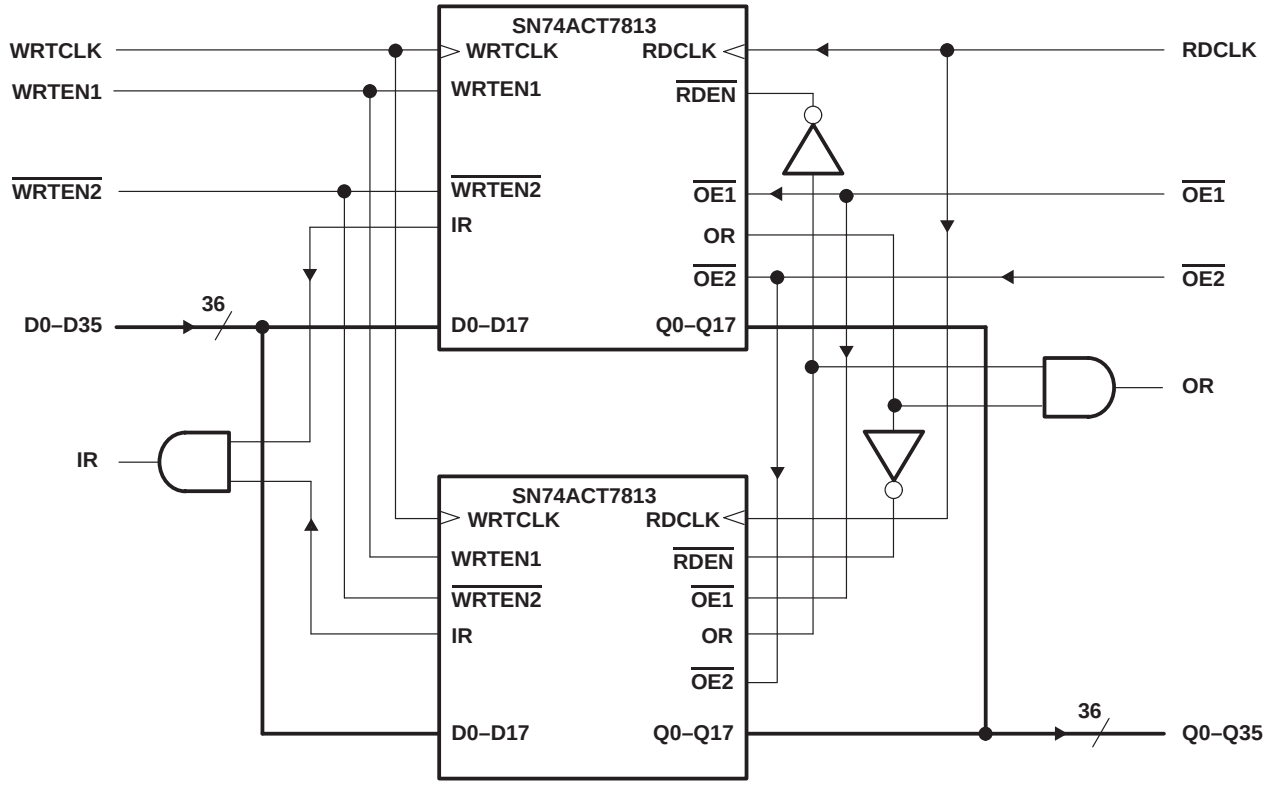


Figure 9. Word-Width Expansion: 64 × 36 Bits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT7813-15DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT7813-15	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

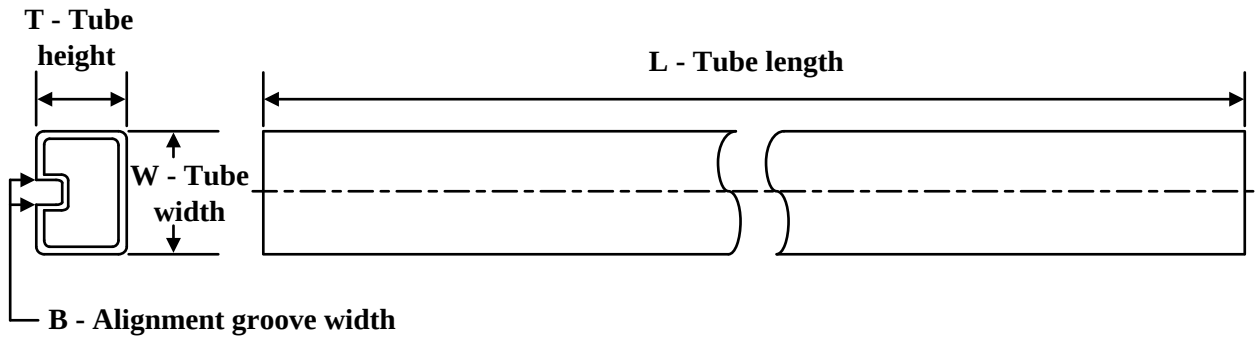
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

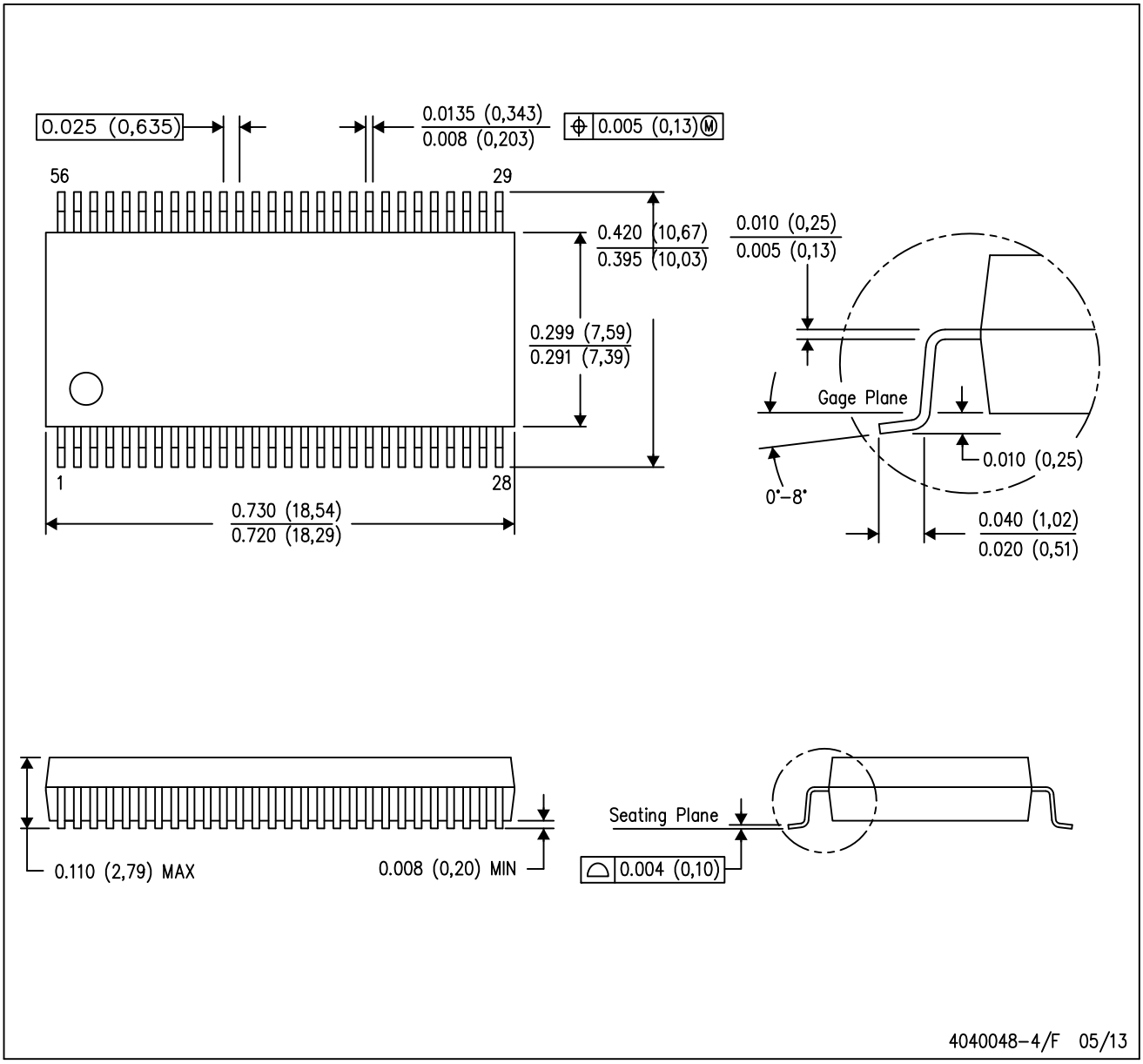
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ACT7813-15DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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