

# 74VHC125FT,74VHC126FT

## 1. Functional Description

- Quad Bus Buffer, Non-Inverted 3-State Outputs
- 74VHC125FT: Quad Bus Buffer  
74VHC126FT: Quad Bus Buffer

## 2. General

The 74VHC125FT,74VHC126FT are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Shottky TTL while maintaining the CMOS low power dissipation.

The 74VHC125FT requires the 3-state control input  $\overline{G}$  to be set high to place the output into the high impedance state, whereas the 74VHC126FT requires the control input G to be set low to place the output into high impedance.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up.

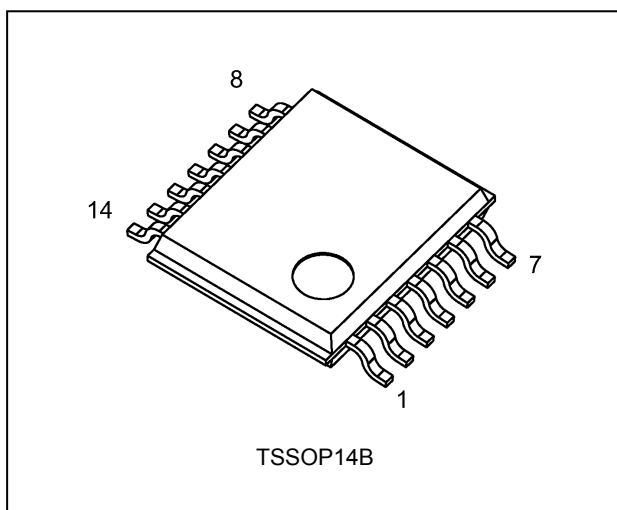
This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature:  $T_{opr} = -40$  to  $125$  °C
- (3) High speed: Propagation delay time = 3.8 ns (typ.) at  $V_{CC} = 5$  V
- (4) Low power dissipation:  $I_{CC} = 4.0$   $\mu$ A (max) at  $T_a = 25$  °C
- (5) High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- (6) Power down protection is provided on all inputs.
- (7) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (8) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  V to 5.5 V
- (9) Low noise:  $V_{OLP} = 0.8$  V (max)
- (10) Pin and function compatible with 74 series (AC/HC/AHC/LV etc.) 125 or 126 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

## 4. Packaging

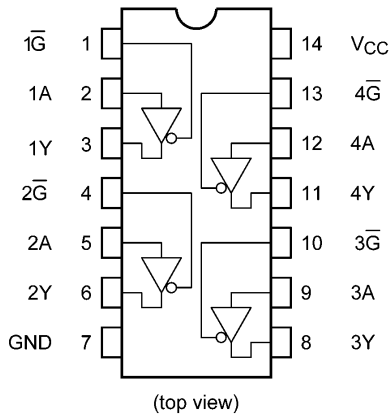


Start of commercial production

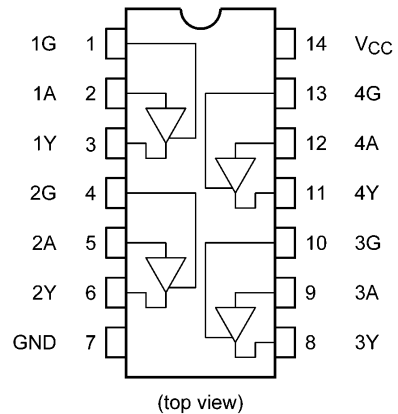
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**5. Pin Assignment**

74VHC125FT

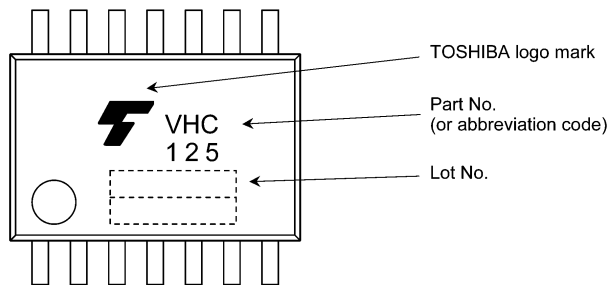


74VHC126FT

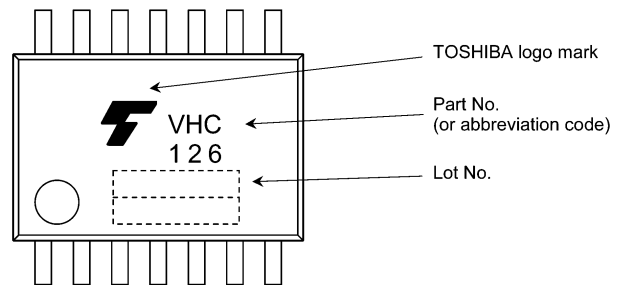


**6. Marking**

74VHC125FT

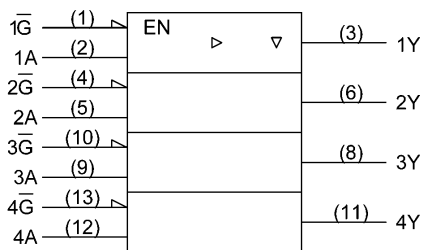


74VHC126FT

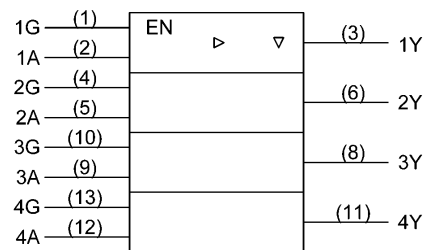


**7. IEC Logic Symbol**

74VHC125FT



74VHC126FT



**8. Truth Table**

Input $\bar{G}$ (74VHC125FT)	Input G (74VHC126FT)	Input An	Output Yn
H	L	X	Z
L	H	L	L
L	H	H	H

X: Don't care  
Z: High impedance

**9. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to 7.0	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		-20	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of  $T_a = -40$  to  $85^{\circ}C$ . From  $T_a = 85$  to  $125^{\circ}C$  a derating factor of  $-3.25$  mW/ $^{\circ}C$  shall be applied until 50 mW.

**10. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage	$V_{IN}$		0 to 5.5	V
Output voltage	$V_{OUT}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 125	$^{\circ}C$
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

**11. Electrical Characteristics**

**11.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
$I_{OH} = -8\text{ mA}$	4.5	3.94		—	—			
	Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1
3.0					—	0.0	0.1	
4.5					—	0.0	0.1	
$I_{OL} = 4\text{ mA}$				3.0	—	—	0.36	
				$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5		—	—	$\pm 0.25$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	$\mu\text{A}$	

**11.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
$I_{OH} = -8\text{ mA}$	4.5	3.80		—			
	Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1
3.0					—	0.1	
4.5					—	0.1	
$I_{OL} = 4\text{ mA}$				3.0	—	0.44	
				$I_{OL} = 8\text{ mA}$	4.5	—	0.44
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5		—	—	$\pm 2.50$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	40.0	$\mu\text{A}$

**11.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125$  °C)**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V	
				3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V	
				3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	—	V	
				3.0	2.9	—		
				4.5	4.4	—		
				$I_{OH} = -4$ mA	3.0	2.40		—
			$I_{OH} = -8$ mA	4.5	3.70	—		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0.1	V	
				3.0	—	0.1		
				4.5	—	0.1		
				$I_{OL} = 4$ mA	3.0	—		0.55
				$I_{OL} = 8$ mA	4.5	—		0.55
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	$\pm 10.0$	$\mu A$	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	$\pm 2.0$	$\mu A$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	80.0	$\mu A$	

**11.4. AC Characteristics (Unless otherwise specified,  $T_a = 25$  °C, Input:  $t_r = t_f = 3$  ns)**

Characteristics	Part Number	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit	
Propagation delay time	74VHC125FT	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	5.6	8.0	ns	
						50	—	8.1	11.5		
					$5.0 \pm 0.5$	15	—	3.8	5.5		
		74VHC126FT	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	5.6	8.0	ns
	50						—	8.1	11.5		
	$5.0 \pm 0.5$					15	—	3.8	5.5		
						50	—	5.3	7.5		
3-state output enable time		$t_{PZL}, t_{PZH}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	—	5.4	8.0	ns	
						50	—	7.9	11.5		
					$5.0 \pm 0.5$	15	—	3.6	5.1		
					50	—	5.1	7.1			
3-state output disable time		$t_{PLZ}, t_{PHZ}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	—	9.5	13.2	ns	
					$5.0 \pm 0.5$	50	—	6.1	8.8		
Output skew		$t_{oS LH}, t_{oS HL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	—	1.5	ns	
					$5.0 \pm 0.5$	50	—	—	1.0		
Input capacitance		$C_{IN}$		—			—	4	10	pF	
Output capacitance		$C_{OUT}$		—			—	6	—	pF	
Power dissipation capacitance	74VHC125FT	$C_{PD}$	(Note 2)	—			—	14	—	pF	
	74VHC126FT						—	15	—		

Note 1: Parameter guaranteed by design. ( $t_{oS LH} = |t_{PLHM} - t_{PLHN}|$ ,  $t_{oS HL} = |t_{PHLM} - t_{PHLN}|$ )

Note 2:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4 \text{ (per gate)}$$

**11.5. AC Characteristics**

(Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Part Number	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time	74VHC125FT	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	9.5	ns
						50	1.0	13.0	
					$5.0 \pm 0.5$	15	1.0	6.5	
						50	1.0	8.5	
	74VHC126FT	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	9.5	ns
						50	1.0	13.0	
					$5.0 \pm 0.5$	15	1.0	6.5	
						50	1.0	8.5	
3-state output enable time		$t_{PZL}, t_{PZH}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	1.0	9.5	ns
						50	1.0	13.0	
					$5.0 \pm 0.5$	15	1.0	6.0	
						50	1.0	8.0	
3-state output disable time		$t_{PLZ}, t_{PHZ}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	1.0	15.0	ns
					$5.0 \pm 0.5$	50	1.0	10.0	
Output skew		$t_{osLH}, t_{osHL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	1.5	ns
					$5.0 \pm 0.5$	50	—	1.0	
Input capacitance		$C_{IN}$		—			—	10	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHM} - t_{PLHN}|$ ,  $t_{osHL} = |t_{PHLM} - t_{PHLN}|$ )

**11.6. AC Characteristics**

(Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)

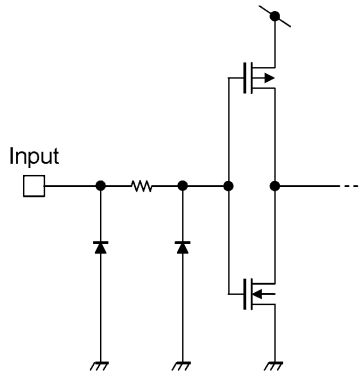
Characteristics	Part Number	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time	74VHC125FT	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	11.0	ns
						50	1.0	14.5	
					$5.0 \pm 0.5$	15	1.0	7.5	
						50	1.0	9.5	
Propagation delay time	74VHC126FT	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	11.0	ns
						50	1.0	14.5	
					$5.0 \pm 0.5$	15	1.0	7.5	
						50	1.0	9.5	
3-state output enable time		$t_{PZL}, t_{PZH}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	1.0	11.0	ns
						50	1.0	14.5	
					$5.0 \pm 0.5$	15	1.0	7.0	ns
						50	1.0	9.0	
3-state output disable time		$t_{PLZ}, t_{PHZ}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	1.0	16.5	ns
					$5.0 \pm 0.5$	50	1.0	11.0	
Output skew		$t_{osLH}, t_{osHL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	1.5	ns
					$5.0 \pm 0.5$	50	—	1.0	
Input capacitance		$C_{IN}$		—			—	10	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHM} - t_{PLHN}|$ ,  $t_{osHL} = |t_{PHLM} - t_{PHLN}|$ )

**11.7. Noise Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

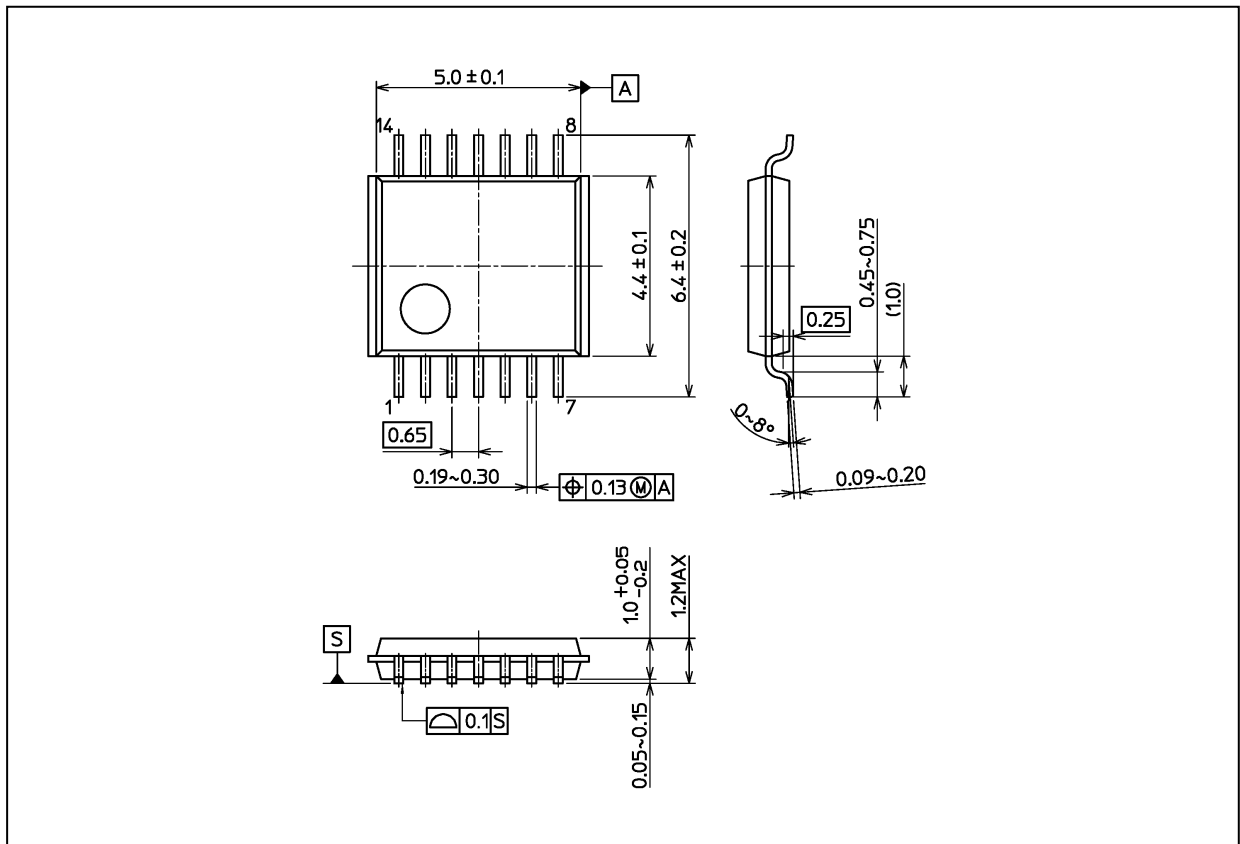
Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$C_L = 50\text{ pF}$	5.0	0.3	0.8	V
Quiet output minimum dynamic $V_{OL}$	$V_{OLV}$	$C_L = 50\text{ pF}$	5.0	-0.3	-0.8	V
Minimum high-level dynamic input voltage	$V_{IHD}$	$C_L = 50\text{ pF}$	5.0	—	3.5	V
Maximum low-level dynamic input voltage	$V_{ILD}$	$C_L = 50\text{ pF}$	5.0	—	1.5	V

**12. Internal Equivalent Circuit**



**Package Dimensions**

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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