PCN Number:	20180924000.0	PCN Date:	October 03, 2018
Title:	Datasheet for DS90UB936-Q1, DS90UB953-Q1, DS90UB954-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DS90UB936-Q1

SNLS571B – MARCH 2018 – REVISED SEPTEMBER 2018

Changes from Revision A (April 2018) to Revision B **Page**

- Added discrete synch signals requirement when using DVP format 28
- Changed FPD3_PCLK to f_{PCLK} in the RAW mode line rate calculations 28
- Added information about YUV support 28
- Relaxed REFCLK Oscillator jitter specification to 200 ps maximum 29
- Relaxed REFCLK Oscillator rise and fall time to 6 ns maximum 29
- Added REFCLK spread-spectrum modulation percentage and frequency 29
- Updated Forward Channel GPIO typical latency value 38
- Updated Back Channel GPIO typical latency and jitter for 50 Mbps rate 38
- Added need for discrete synch signals in DVP mode and included RAW/YUV support 41
- Changed from GPIO7 pin to GPIO6 pin 46
- Deleted sentence "It is recommended to forward the relevant RX port data streams prior to enabling the 48
- CSI-2 TX output"..... 48
- Added Enabling and Disabling the CSI-2 Transmitter section 48
- Changed Node VDDIO to VI2C for SCL and SDA signal lines 56
- Added sentence about RX port specific register for registers 0x4A, 0x4B, 0x4D - 0x7F, 0xD0 - 0xDF 92
- Updated RX_PORT_STS2 register bit 1 field and description 95
- Changed PAR_ERROR line _BYTE_1 to PAR_ERROR _BYTE_1 and RX PARITY CHECKER ENABLE to RX_PARITY_CHECKER_ENABLE 97
- Redraw the PoC Network diagram 138
- Updated Return Loss S11 values 140
- Redraw RINx STP setting for figure "Typical Connection Diagram STP With External 1.1-V supply"..... 142

TEXAS INSTRUMENTS

DS90UB953-Q1

SNLS552B – SEPTEMBER 2017 – REVISED SEPTEMBER 2018

Changes from Revision A (February 2018) to Revision B	Page
• Updated GPIO pin descriptions.	6
• Replace CLK_IN with clock throughout document.	6
• Changed Supply voltage from 2.5V to 2.16V	7
• Changed asynchronous to non-synchronous	8
• Deleted "for synchronous mode"	8
• Added internal reference frequency in EC table	10
• Added Internal AON Clock to Block Diagram.	15
• Changed mode to modes.	18
• Changed 130ns to 225ns.	22
• Changed latency to 1.5us and jitter to 0.7us.	22
• Changed CLK_IN Mode to Modes.	22
• Added DVP Mode	22
• Changed table formatting.	23
• Changed REFLCK to Back Channel	23
• Added Frequency for Synchronous Mode	23
• Changed naming convention from "asynchronous CLK_IN" to "Non-Synchronous external CLK_IN" mode column dor CLKIN_DIV = 2	23
• Changed from CLK_IN to Back Channel (Half Rate).	23
• Added Non-Synchronous Internal Clock Mode	23
• Changed the value from 24.2 - 25.5 MHz to 48.4 - 51 MHz	23
• Changed the value from 25 - 52 MHz to 24.2 to 25.5 MHz	23
• Added DVP External Clock.	23
• Added text "Deserializer Mode" to clarify mode RAW10	23
• Added additional information to note.	23
• Added text "Deserializer Mode" to clarify mode RAW12 HF	23
• Changed CLK_IN to Clock.	23
• Added Non-Synchronous Internal Clocking Mode section.	24
• Changed the internal clock 25 MHz to 24.2 MHz	24
• Changed forward channel rate to1.936 Gbps instead of 2 Gbps	24
• Changed the average CSI-2 throughput value to 3.1 Gbps instead of 1.6 Gbps	24
• Added DVP Backwards Compatibility Mode section.	24
• Changed "asynchronous CLK_IN" to "Non-Synchronous external CLK_IN"	25
• Added sentence "CLK_OUT functionality is not..."	25
• Added Non-Synchronous Internal Clock Mode	26
• Deleted "with accuracy of 25 MHz ±10%.	28
• Changed clock to from 25 MHz ±10% to 26.25 MHz.	28
• Changed clock to from 25 MHz ±10% to 26.25 MHz.	28
• Updated registers map	32
• Added information for DVP mode to register 0x04.	33
• Added "operating with Non-Synchronous internal clock or"	34
• Changed the frequency value from 26 MHz to range value (24.2 MHz to 25.5 MHz)	34
• Added "set for 2 Gbps line rate"	34
• Changed the frequency value from 52 MHz to range value (48.4 MHz to 51 MHz)	34
• Added "set for 4 Gbps line rate"	34
• Updated unit time and clock frequency.	36
• Added DVP information to register 0x10.	37
• Added DVP information to register 0x11.	37
• Deleted the value -25dB and added -20dB in typcial	71
• Changed –26.4+14.4f to log equation –12+8*log(f)	71
• Moved Return Loss, S11 MAX values to TYP	71
• Added Typical connection diagram for STP	72
• Changed the capacitance value from 33nF to 33nF – 100 nF.	73
• Changed the capacitance value from 15 nF to 15 nF – 47 nF	73
• Changed the capacitance value from 33nF to 33nF – 100 nF.	73

Changes from Original (August 2017) to Revision A **Page**

- Changed supply voltage test condition from V(VDD11)(VDD_SEL = LOW ONLY to V(VDD11)(VDD_SEL = HIGH ONLY) 8
- Added spread-spectrum reference clock modulation percentage parameter to the ROC tables 9
- Added V(VDDIO) VDD18 ±50mV test condition to the high level output voltage parameter 11
- Added V(VDDIO) = VDD18 ±50mV test to the low level output voltage parameter 11
- Added PDB pin/frequency test condition and values to the high level input voltage parameter 12
- Added PDB pin/frequency test condition and values to the low level input voltage parameter 12
- Changed output short circuit current symbol from Isc to Ios 12
- Added AEQ rating ±3ms RAW mode to the deserializer data lock time parameter 13
- Added data bit rate minimum and typical values to the REFCLK = 23 MHz and REFCLK = 26 MHz test conditions 14
- Added DDR clock frequency minmum and typical values to the REFCLK = 23 MHz and REFCLK = 26 MHz test conditions 14
- Added the text '1.5 Gbps' after the 'Data rate <' and 'Data rate >' text in slew rate test conditions for falling and rising edge 16
- Changed the UI instantaneous maximum value from 12.5 ns to 2.7 ns 16
- Added discrete synch signals requirement when using DVP format 28
- Changed FPD3_PCLK to f_{PCLK} in the RAW mode line rate calculations 28
- Added information about YUV support 28
- Removed Coax/STP column and reorganized rows. 29
- Relaxed REFCLK Oscillator jitter specification to 200 ps maximum 29
- Relaxed REFCLK Oscillator rise and fall time to 6 ns maximum 29
- Added REFCLK spread-spectrum modulation percentage and frequency 29
- Changed Text from: AEQ_FLOOR value to: ADAPTIVE_EQ_FLOOR_VALUE 33

- Updated Forward Channel GPIO typical latency value 39
- Updated Back Channel GPIO typical latency and jitter for 50 Mbps rate 39
- Added need for discrete synch signals in DVP mode and included RAW/YUV support 42
- Changed from GPIO7 pin to GPIO6 pin 47
- Changed Text from: The total period of the FrameSync is (1 s / 60 hz) / 600 ns to: The total period of the FrameSync is (1 / 60 hz) / 600 ns 48
- Deleted Sentence "It is recommended to forward the relevant RX port data streams prior to enabling the CSI-2 TX output" 49
- Added Enabling and Disabling the CSI-2 Transmitter section 49
- Changed Sensor A and B to Sensor X in definition list 51
- Changed Node VDDIO to VI2C for SCL and SDA signal lines 57
- Changed Register 0x7C to register 0x7D 67
- Changed BIST_CTL to BIST Control to match register map 71
- Changed Parity Error Threshold High to PAR_ERR_THOLD_HI 74
- Changed Parity Error Threshold Low to PAR_ERR_THOLD_LO 74
- Added Cross-reference to GPIO4_OUT_SRC bit description 80
- Changed GPIO5_OUT_VAL bit description text from: GPIO5_OUT_SEL[2:0] = 00 to: GPIO5_OUT_SEL[2:0] = 000 80
- Changed GPIO6_OUT_VAL bit description text from: GPIO6_OUT_SEL[2:0] = 00 to: GPIO6_OUT_SEL[2:0] = 000 80
- Changed FS_GEN_MODE bit description text from: 'FS_HIGH_TIME and FS_LOW_TIME register values' to: 'FS_HIGH_TIME [15:0] and FS_LOW_TIME [15:0] register values' for clarity 81
- Changed INT bit to INTERRUPT_STS bit in INTERRUPT_STS bit description 85
- Changed RESERVED bit numbers from: 6:4 to: 6:5 85
- Changed RESERVED bit description text from: CSI_PLL to: CSI_PLL_CTL 88
- Added sentence about RX port specific register for registers 0x4A, 0x4B, 0x4D - 0x7F, 0xD0 - 0xDF 94
- Updated RX_PORT_STS2 register bit 1 field and description 97
- Changed VOLT1_SENSE_LEVEL to VOLT0_SENSE_LEVEL 98
- Changed PAR_ERROR line _BYTE_1 to PAR_ERROR _BYTE_1 and RX PARITY CHECKER ENABLE to RX_PARITY_CHECKER_ENABLE 99
- Changed RX PARITY CHECKER ENABLE to RX_PARITY_CHECKER_ENABLE 99
- Changed BCC_Config Register 0x58[2:0] binary setting value from 0b100 to 0b010 to select 10 Mbps non-synchronous back channel rate. 100

- Removed Text 'This field is normally loaded from the remote serializer. It can be overwritten if the OVERRIDE_FC_CONFIG bit in the DATAPATH_CTL0 register is 1.' from the RESERVED bit description 101
- Changed PASSPARITY-ERR to PASS_PARITY_ERR 114
- Removed Broken link in the IND_ACC_CTL register table 116
- Changed IA_SEL bit enumerations from: 0001-0100 and 1000-0111 to: 00011–0100 and 1000–1111 116
- Changed RESERVED Register to FPD3_ENC_CTL 118
- Changed RESERVED bit numbers from: 5:3 to: 4:2 119
- Changed ADAPTIVE_EQ_FLOOR_VALUE bit description from: register {reg_35[5:4]} to: register 0xD2[2] 122
- Changed IE_FC_SENS_STS bit description from: Camera and CAM to: Sensor and SEN 124
- Fixed Broken link in *Power Over Coax* section 139
- Redraw the PoC Network diagram 140
- Updated Return Loss S11 values 142
- Redraw RINx STP setting for figure "Typical Connection Diagram STP With External 1.1-V supply" 144
- Fixed Broken links in the *Detailed Design Procedure* section 145
- Removed Second paragraph in *System Examples* 146

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UB936-Q1	SNLS571A	SNLS571B
DS90UB953-Q1	SNLS552A	SNLS552B
DS90UB954-Q1	SNLS570	SNLS570A

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DS90UB936-Q1

http://www.ti.com/product/DS90UB953-Q1

http://www.ti.com/product/DS90UB954-Q1

Reason for Change:
To accurately reflect device characteristics.
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):
No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.
Changes to product identification resulting from this PCN:
None.
Product Affected:

DS90UB936TRGZRQ1	DS90UB936TRGZTQ1	DS90UB953TRHBRQ1	DS90UB953TRHBTQ1
DS90UB954TRGZRQ1	DS90UB954TRGZTQ1		

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	**E-Mail**
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com