SN65HVD1781A-Q1 Fault-Protected RS-485 Transceivers With 3.3-V to 5-V Operation

1 Features

- Qualified for automotive applications
- AEC-Q100 Qualified with the following results
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESG classification level C3B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Bus-pin fault protection to: > ±70 V
- Operation with 3.3-V to 5-V supply range
- ±16-kV HBM protection on bus pins
- Reduced unit load for up to 320 nodes
- Failsafe receiver for open-circuit, short-circuit and idle-bus conditions
- Low power consumption
  - Low standby supply current, 1 µA maximum
  - I_{CC} 4-mA Quiescent during operation
- Pin-compatible with industry-standard SN75176
- Signaling rates up to 1 Mbps

2 Applications

- Infotainment, clusters
- HMI and displays
- Media interface
- Head unit

3 Description

The device is designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. It is also robust to ESD events, with high levels of protection to the human-body-model specification.

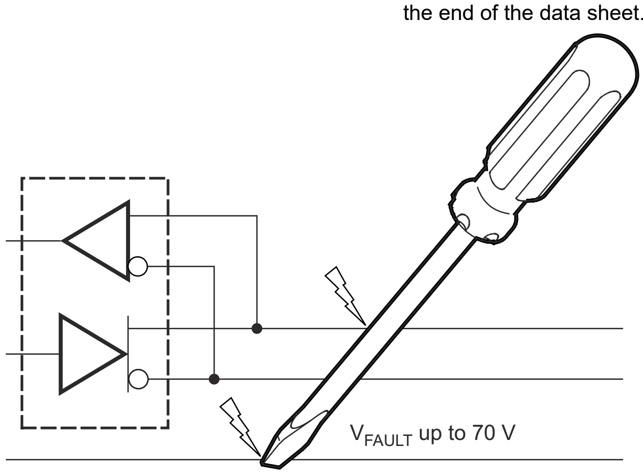
The SN65HVD1781A-Q1 combines a differential driver and a differential receiver, which operate from a single power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the device suitable for multipoint applications over long cable runs. The device is characterized from –40°C to 125°C. The SN65HVD1781A-Q1 device is pin-compatible with the industry-standard SN75176 transceiver, making it a drop-in upgrade in most systems.

The device is fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications. For applications where operation is required over an extended common-mode voltage range, see the SN65HVD1785 (SLLS872) data sheet.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65HVD1781A-Q1	SOIC	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2017) to Revision A (February 2022)	Page
• Added *Feature* Functional Safety-Capable	1

5 Pin Configuration and Functions

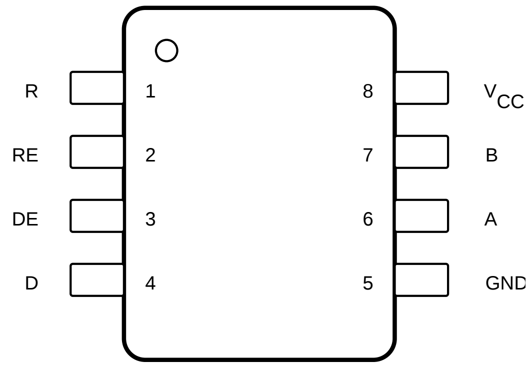


Figure 5-1. D (SOIC) Package, 8-Pin, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	3.15-V-to-5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

See Note [(1)].

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
	Voltage range at bus pins	A, B pins	–70	70	V
	Input voltage range at any logic pin		–0.3	V_{CC} + 0.3	V
	Transient overvoltage pulse through 100 Ω per TIA-485		–70	70	V
	Receiver output current		–24	24	mA
	Continuous total power dissipation		See *Section 6.7*		
T_J	Junction temperature			170	°C
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—AEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	Bus terminals and GND	±16000	V
			All pins	±4000	
		Charged-device model (CDM), per AEC Q100-011		±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per IEC 60749-26	Bus terminals and GND	±16000	V

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)[(1)]		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate				1	Mbps
T_A	Operating free-air temperature (See the *Section 6.5* table)	5-V supply	–40		105	°C
		3.3-V supply	–40		125	
T_J	Junction Temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

6.5 Thermal Information

THERMAL METRIC[(1)]			SN65HVD1781A-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	JEDEC high-K model	97.7	°C/W
		JEDEC low-K model	242	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		39.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		38.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V, See Figure 7-1	T_A < 85°C	1.5			V
			T_A < 125°C	1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V	T_A < 85°C	1.7	2		
			T_A < 125°C	1.5			
		R_L = 54 Ω, 3.15 V ≤ V_{CC} ≤ 3.45 V		0.8	1		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V	T_A < 85°C	2.2	2.5		
			T_A < 125°C	2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω		–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage			1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage			–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 7-2			500		mV
C_{OD}	Differential output capacitance				23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				–100	–35	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–180	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$)(1)			30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	T_A < 85°C		0.2	0.4	V
			T_A < 125°C			0.5	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current			–50		50	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_{OS}	Driver short-circuit output current			–200		200	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V		75	100	µA
			V_I = –7 V	–60	–40		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load		4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load		3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load		2	4	
		Driver and receiver disabled, standby mode	DE = GND, D = open, RE = V_{CC}, no load, T_A < 85°C		0.15	1	µA
			DE = GND, D = open, RE = V_{CC}, no load, T_A < 125°C			12	
	Supply current (dynamic)	See the *Section 6.9* section					

(1) Ensured by design. Not production tested.

6.7 Power Dissipation Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Power dissipation	V_{CC} = 3.6 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, unterminated[1]	75	mW
		V_{CC} = 3.6 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-422 load[1]	95	
		V_{CC} = 3.6 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 3.3-V supply, RS-485 load[1]	115	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated[1]	290	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load[1]	320	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load[1]	400	
T_{SD}	Thermal-shutdown junction temperature		170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

6.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 7-3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See Figure 7-3				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} – t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See Figure 7-3				25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 7-4 and Figure 7-5				3	μs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 7-4 and Figure 7-5			300	ns
		Receiver disabled				10	μs
RECEIVER							
t_r, t_f	Receiver output rise/fall time [1]	C_L = 15 pF, See Figure 7-6			4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L = 15 pF, See Figure 7-6			100	200	ns
$t_{SK(P)}$	Receiver output pulse skew, $\|t_{PHL} – t_{PLH}\|$	C_L = 15 pF, See Figure 7-6			6	20	ns
t_{PLZ}, t_{PHZ}	Receiver disable time [1]	Driver enabled, See Figure 7-7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 7-7			80	300	ns
		Driver disabled, See Figure 7-8			3	9	μs

(1) Specified by design. Not production tested.

6.9 Typical Characteristics

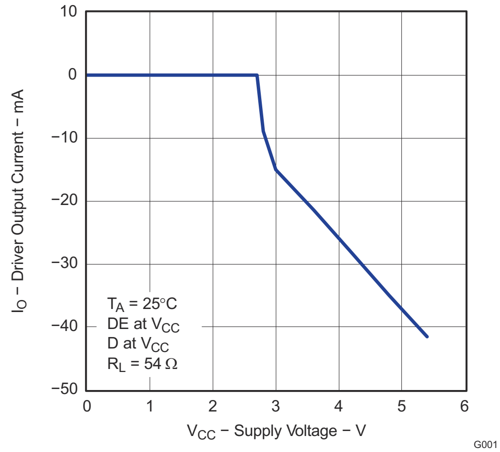


Figure 6-1. Driver Output Current vs Supply Voltage

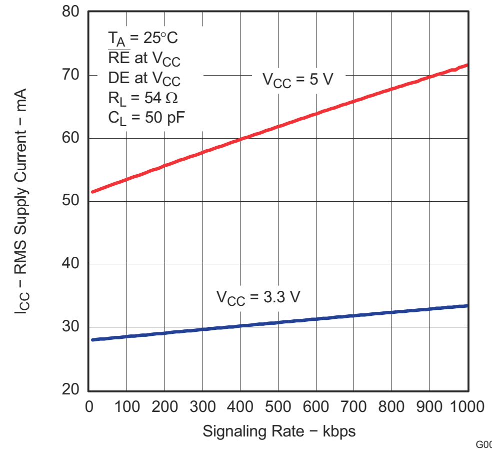


Figure 6-2. RMS Supply Current vs Signaling Rate

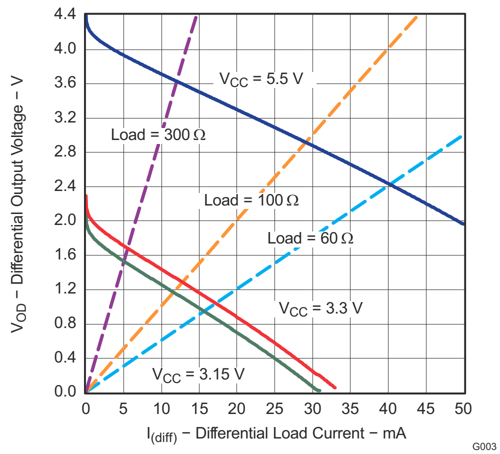


Figure 6-3. Differential Output Voltage vs Differential Load Current

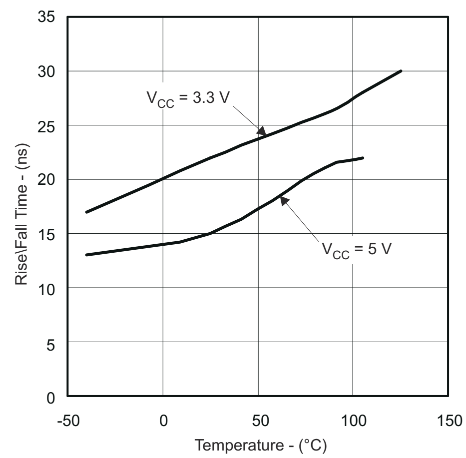


Figure 6-4. Rise and Fall Time

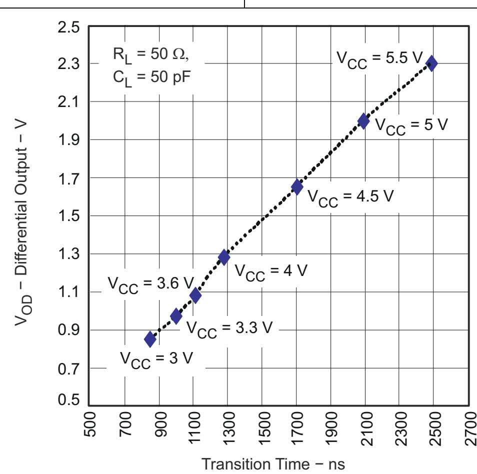


Figure 6-5. Differential Output Amplitude and Transition Time vs Supply Voltage

7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 ns, output impedance 50 Ω.

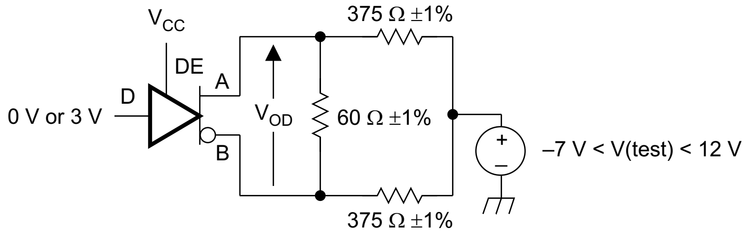


Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

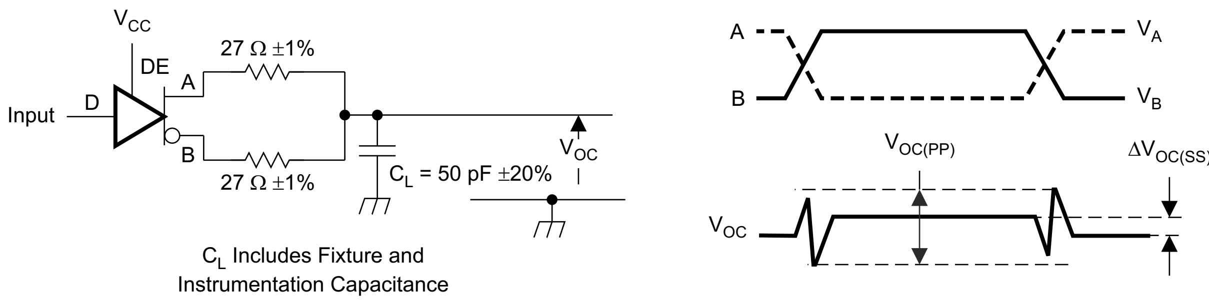


Figure 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

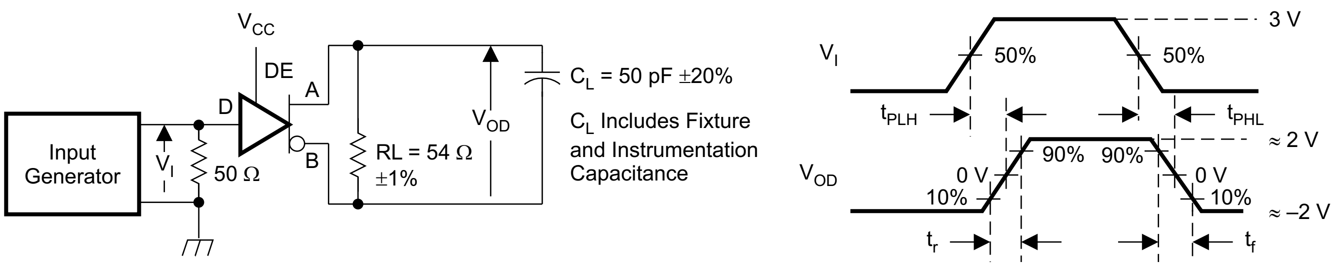
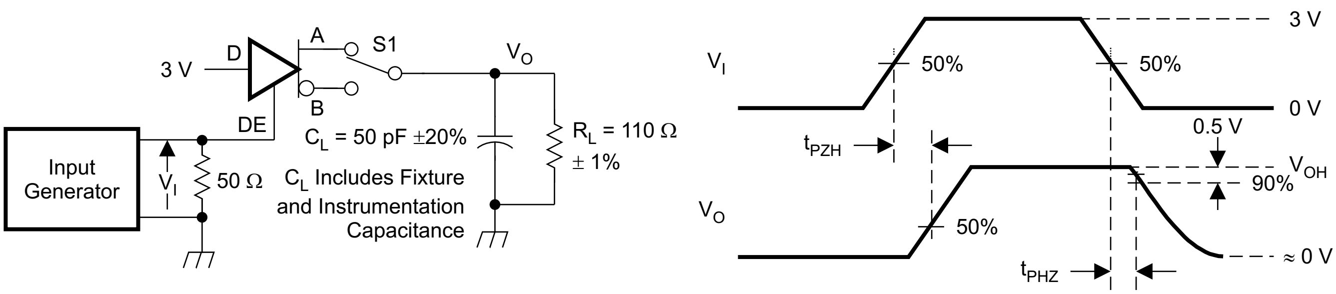
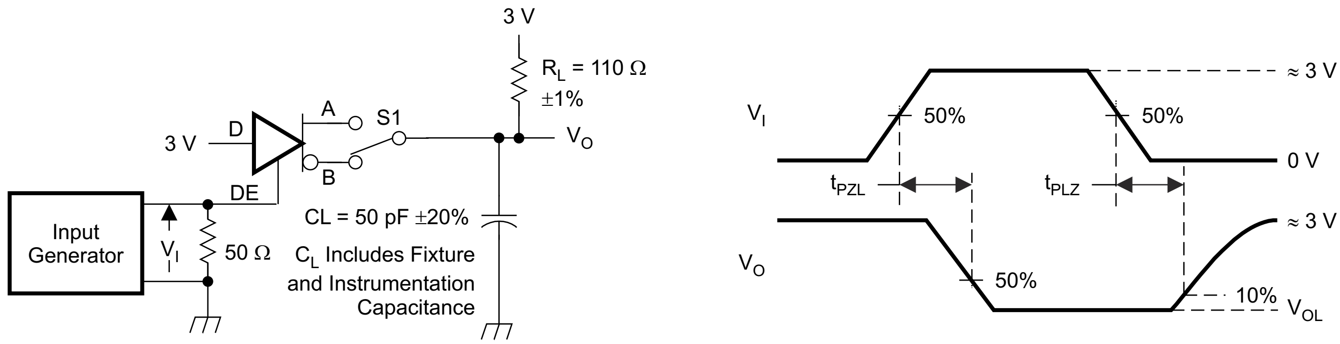


Figure 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 7-5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

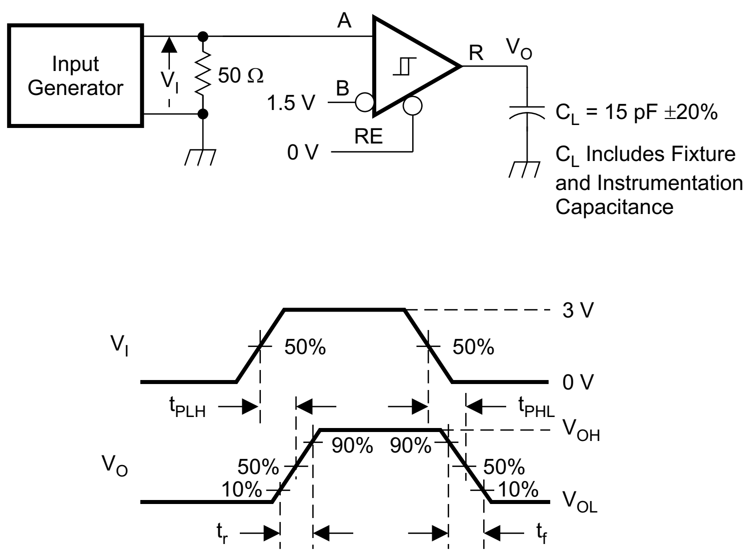


Figure 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

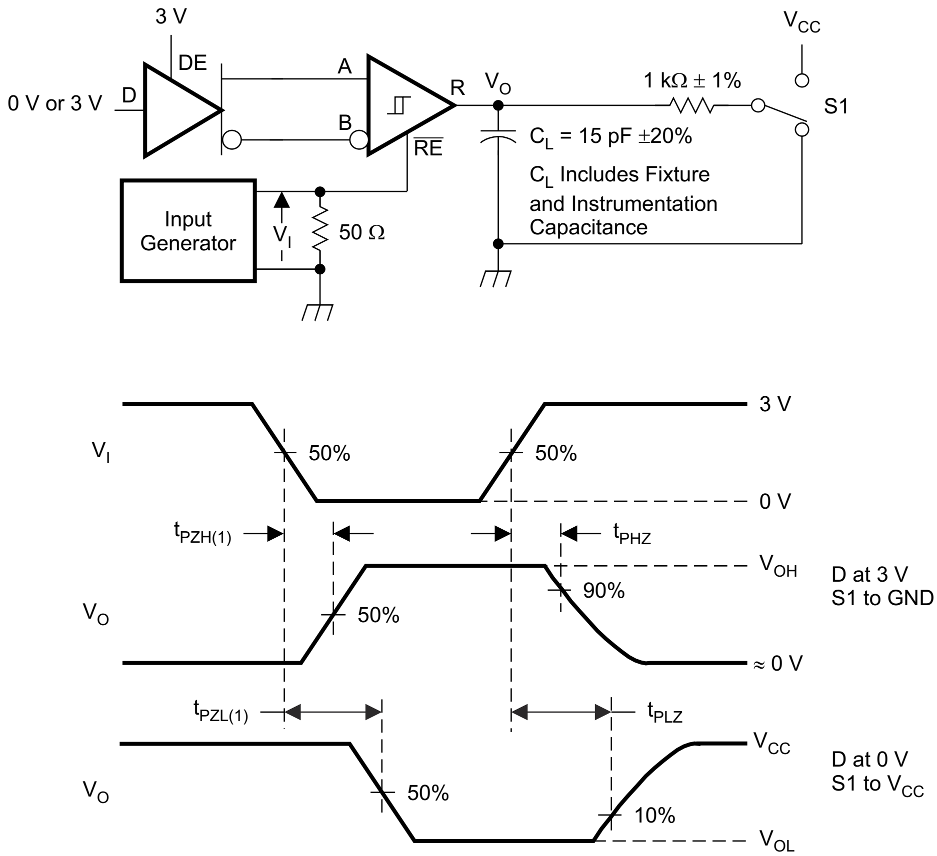


Figure 7-7. Measurement of Receiver Enable and Disable Times With Driver Enabled

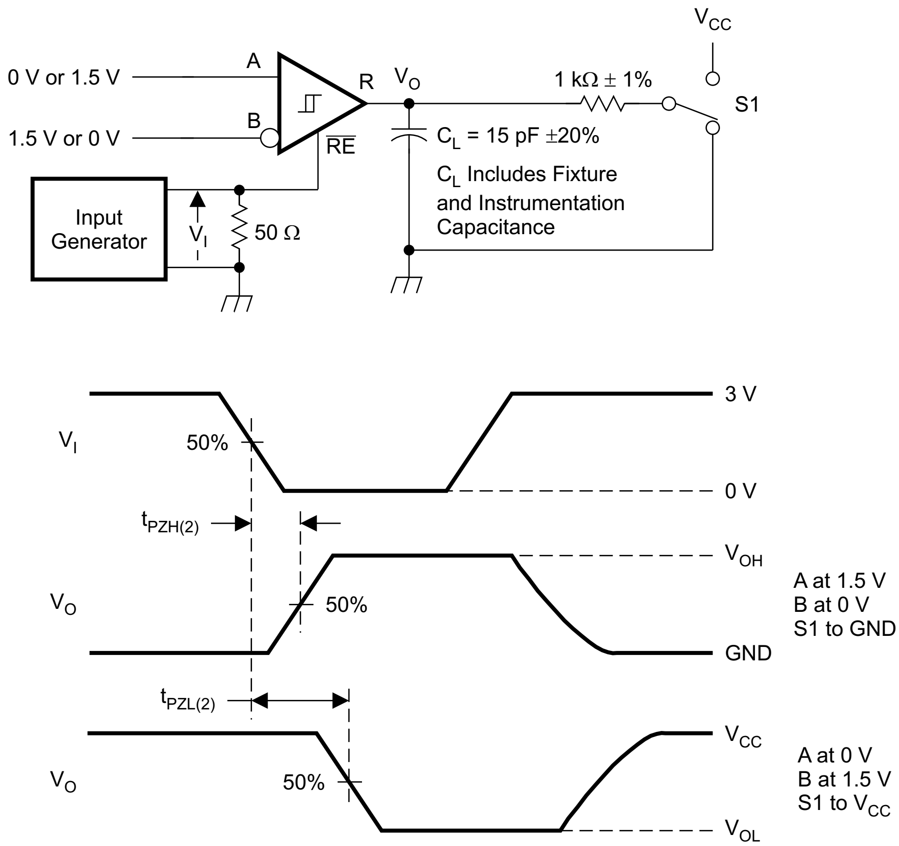


Figure 7-8. Measurement of Receiver Enable Times With Driver Disabled

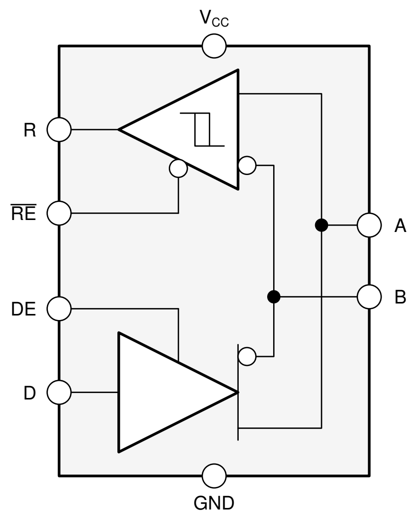
8 Detailed Description

8.1 Overview

The SN65HVD1781A-Q1 is a half-duplex RS-485 transceiver that operates at data rates up to 1 Mbps.

The device features a wide common-mode operating range and bus-pin fault protection up to ±70 V. The device has an active-high driver enable and active-low receiver enable. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagram



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8.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16-kV Human Body Model (HBM) electrostatic discharges.

Device operation is specified over a wide temperature range from –40°C to 125°C.

8.3.1 Receiver Failsafe

The SN65HVD1781A-Q1 half-duplex transceiver provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –35 mV and an input hysteresis of V_{HYS} = 30 mV, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to 130-mV_{PP} differential noise without the need for external failsafe biasing resistors.

8.3.2 Hot-Plugging

The SN65HVD1781A-Q1 is designed to operate in *hot swap* or *hot-pluggable* applications. Key features for hot-pluggable applications are power-up and power-down glitch free operation, default disabled input and output pins, and receiver failsafe.

As shown in the *Section 8.2*, an internal power-on reset circuit keeps the driver outputs in a high impedance state until the supply voltage has reached a level at which the device will reliably operate. This circuit ensures that no problems occur on the bus pin outputs as the power supply turns on or off.

As shown in *Section 8.4*, the driver and receiver enable inputs (DE and $\overline{RE}$) are disabled by default. This default ensures that the device neither drives the bus nor reports data on the R pin until the associated controller actively drivers the enable pins.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		DRIVER STATE
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	RECEIVER STATE
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65HVD1781A-Q1 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

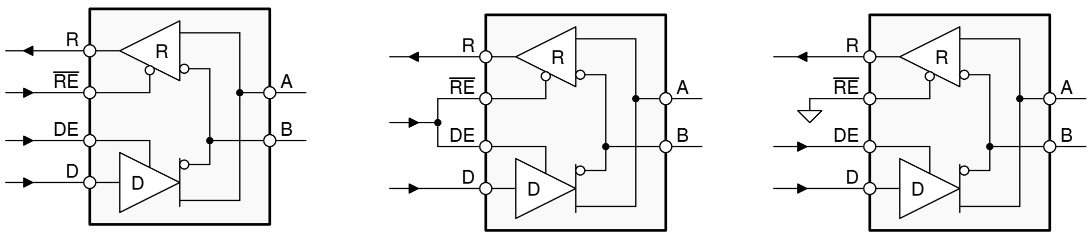


Figure 9-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

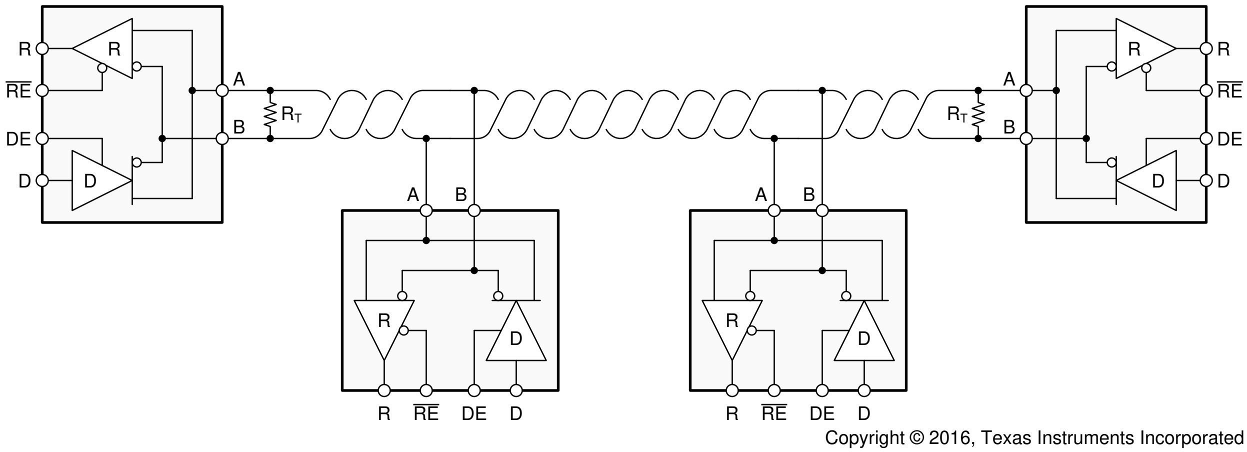


Figure 9-2. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

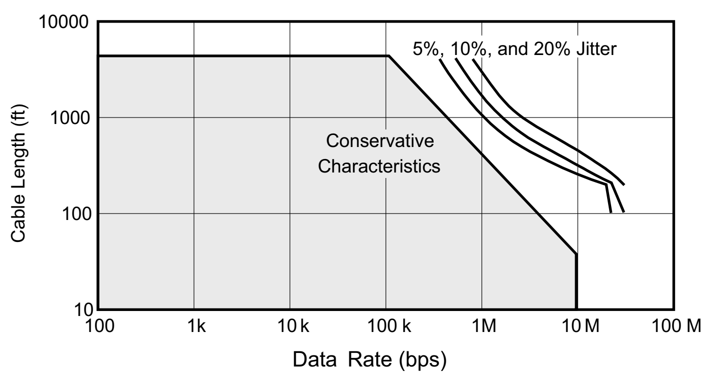


Figure 9-3. Cable Length vs Data Rate Characteristic

9.2.1.2 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD1781A-Q1 consists of 1/10 UL transceivers, it is possible to connect up to 320 receivers to the bus.

9.2.2 Detailed Design Procedure

Although the SN65HVD1781A-Q1 is internally protected against human-body-model ESD strikes up to ±16 kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

Figure 9-4 shows a protection circuit intended to withstand ±8-kV IEC ESD (per IEC 61000-4-2) as well as ±4-kV EFT (per IEC 61000-4-4).

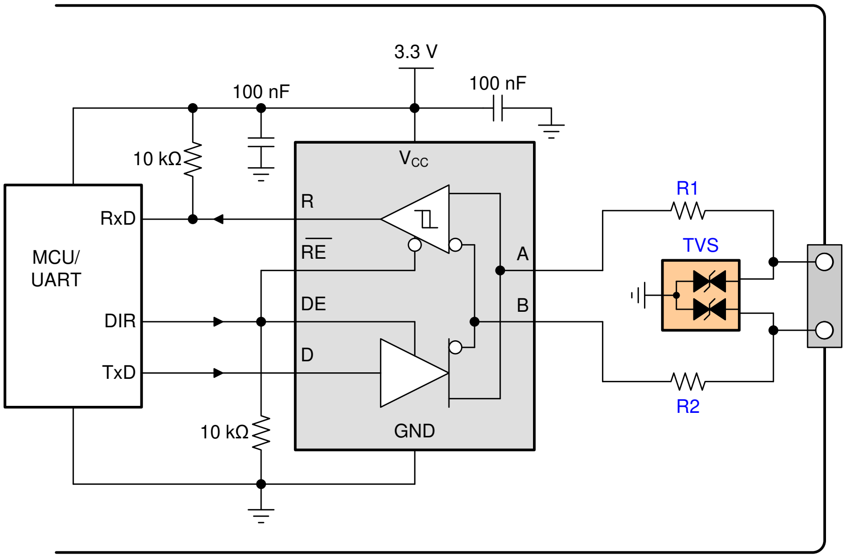


Figure 9-4. RS-485 Transceiver with External Transient Protection

Table 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 Transceiver	SN65HVD1781A-Q1	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 600-W Transient Suppressor	SMBJ43CA	Littelfuse

9.2.2.1 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.2.2 Receiver Failsafe

The differential receivers of the SN65HVD1781A-Q1 has receiver input thresholds that are offset so that receiver output state is known for the following three fault conditions:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$, $V_{IT(–)}$, and V_{HYS} (the separation between $V_{IT(+)}$ and $V_{IT(–)}$). As shown in the *Section 6.6* table, differential signals more negative than –200mV will always cause a Low receiver output, and differential signals more positive than 200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of –35 mV, and the receiver output will be High. Only when the differential input is more than V_{HYS} below $V_{IT(+)}$ will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS}, as well as the value of $V_{IT(+)}$.

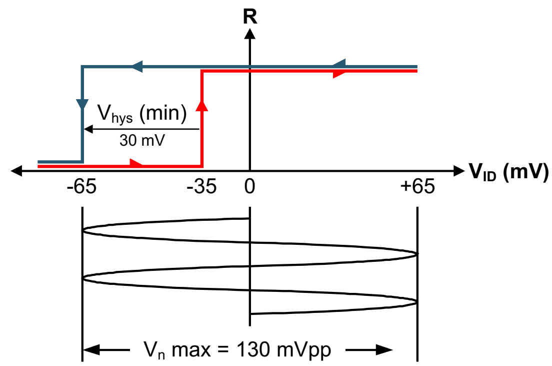
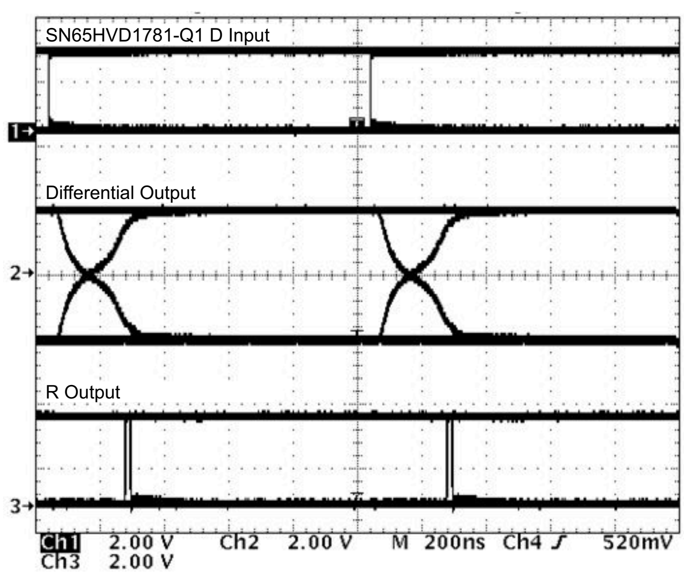


Figure 9-5. Noise Immunity Under Bus Fault Conditions

9.2.3 Application Curve



1-Mbps Operation

Figure 9-6. SN65HVD1781A-Q1 PRBS Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS7A6150-Q1 is a linear voltage regulator suitable for the 5-V supply.

11 Layout

11.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

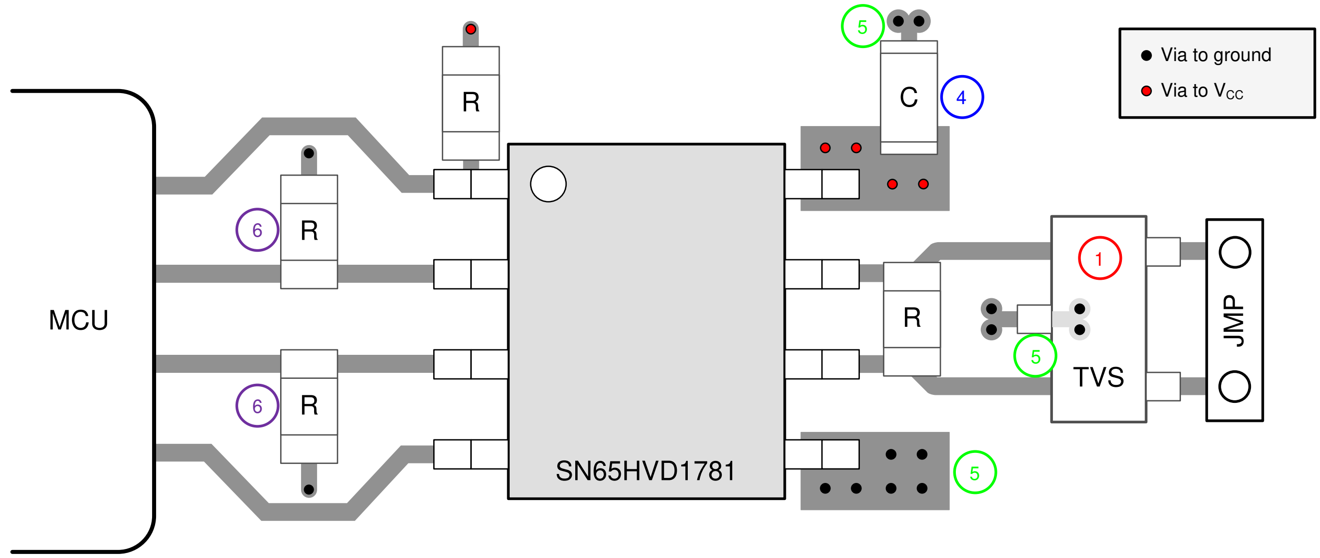


Figure 11-1. Half-Duplex Layout Example

12 Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *RS-485 Half-Duplex Evaluation Module*
- *SN65HVD17xx Fault-Protected RS-485 Transceivers With Extended Common-Mode Range*
- *TPS7A6xxx-Q1 300-mA 40-V Low-Dropout Regulator With 25-μA Quiescent Current*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

12.5 Trademarks

All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1781AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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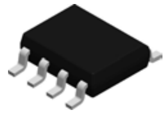
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

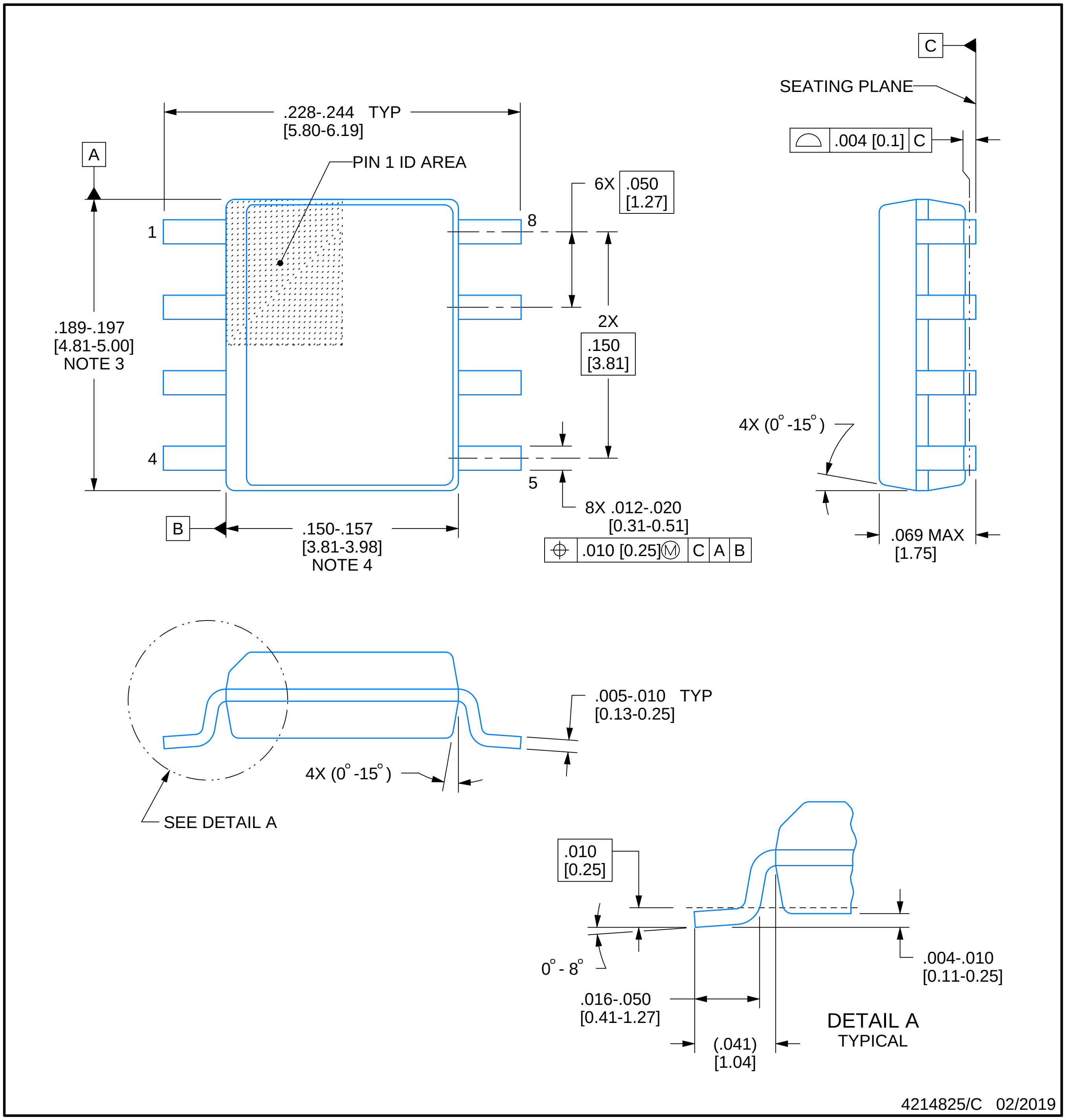


PACKAGE OUTLINE

D0008A

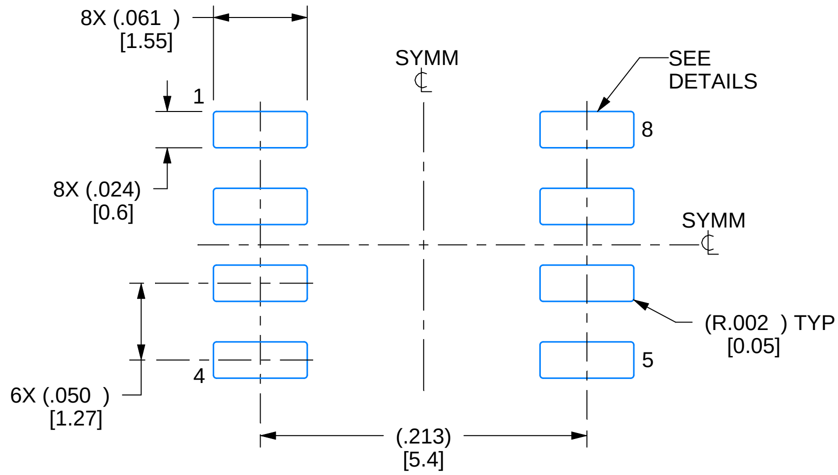
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

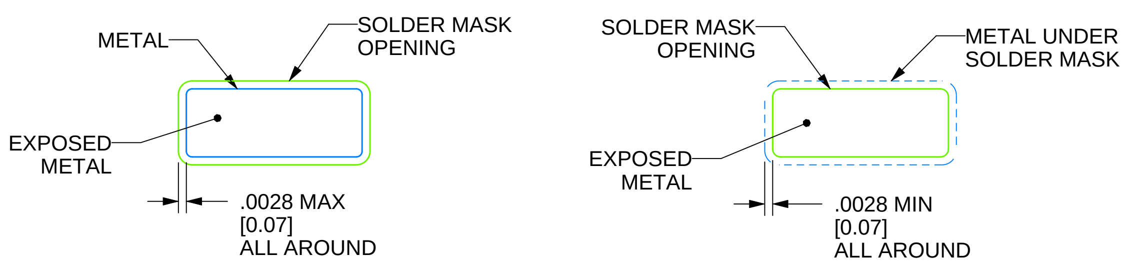


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

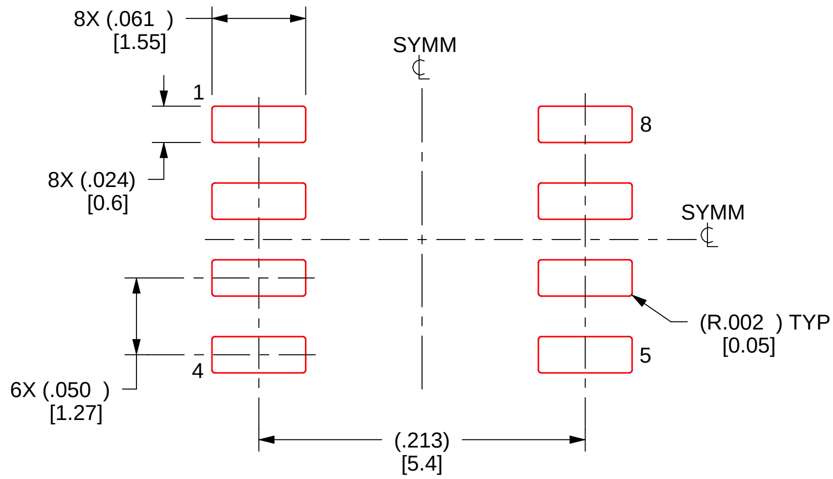
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.