S-1009 Series

0.27 μA CURRENT CONSUMPTION VOLTAGE DETECTOR WITH DELAY FUNCTION (EXTERNAL DELAY TIME SETTING)

© ABLIC Inc., 2009-2017

The S-1009 Series is a super high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally with an accuracy of ±0.5%. It operates with super low current consumption of 270 nA typ.
The release signal can be delayed by setting a capacitor externally. Delay time accuracy is ±15%. Two output forms Nch open-drain and CMOS output are available.
Compared with conventional CMOS voltage detectors, the S-1009 Series is the most suitable for the portable devices due to the super-low current consumption, super high-accuracy and small packages.

■ Features

- Detection voltage: 0.8 V to 4.6 V (0.1 V step)
- Detection voltage accuracy: ±0.5% (2.4 V ≤ $-V_{DET}$ ≤ 4.6 V)
  ±12 mV (0.8 V ≤ $-V_{DET}$ < 2.4 V)
- Current consumption: 270 nA typ. (1.2 V ≤ $-V_{DET}$ < 2.3 V)
- Operation voltage range: 0.6 V to 10.0 V (CMOS output product)
- Hysteresis width: 5% ±1%
- Delay time accuracy: ±15% (C_D = 4.7 nF)
- Output form: Nch open-drain output (active "L")
  CMOS output (active "L")
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

■ Applications

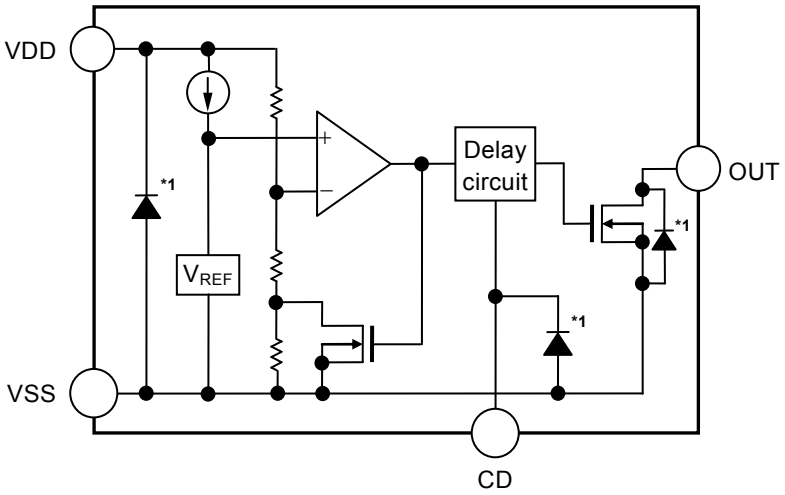
- Power monitor and reset for CPU and microcomputer
- Constant voltage power monitor for TV, DVD recorder and home appliance
- Power supply monitor for portable device such as notebook PC, digital still camera and mobile phone

■ Packages

- SOT-23-5
- SC-82AB
- SNT-4A

■ Block Diagrams

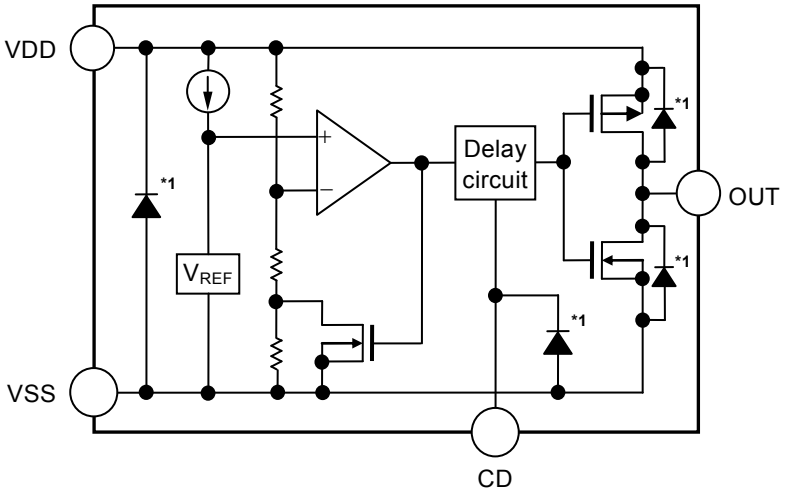
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. CMOS output product



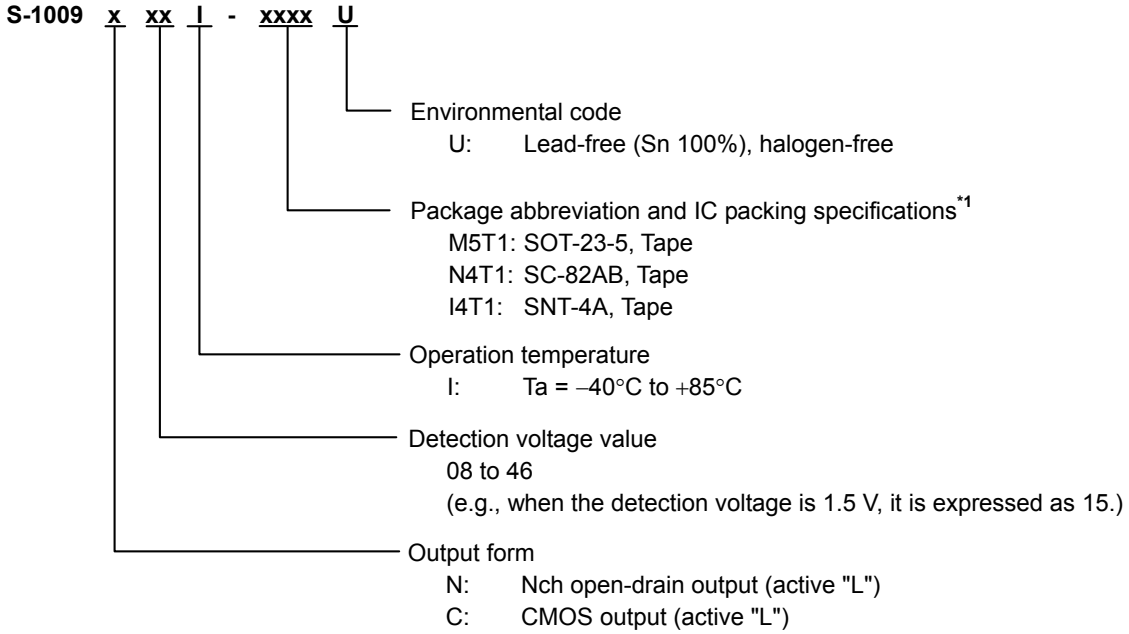
***1.** Parasitic diode

Figure 2

■ Product Name Structure

Users can select the output form, detection voltage value, and package type for the S-1009 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings and "**3. Product name list**" regarding details of product name.

1. Product name



***1.** Refer to the tape drawings.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD	–
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

3. 1 Nch open-drain output product

Table 2

Detection Voltage	SOT-23-5	SC-82AB	SNT-4A
0.8 V ± 12 mV	S-1009N08I-M5T1U	S-1009N08I-N4T1U	S-1009N08I-I4T1U
0.9 V ± 12 mV	S-1009N09I-M5T1U	S-1009N09I-N4T1U	S-1009N09I-I4T1U
1.0 V ± 12 mV	S-1009N10I-M5T1U	S-1009N10I-N4T1U	S-1009N10I-I4T1U
1.1 V ± 12 mV	S-1009N11I-M5T1U	S-1009N11I-N4T1U	S-1009N11I-I4T1U
1.2 V ± 12 mV	S-1009N12I-M5T1U	S-1009N12I-N4T1U	S-1009N12I-I4T1U
1.3 V ± 12 mV	S-1009N13I-M5T1U	S-1009N13I-N4T1U	S-1009N13I-I4T1U
1.4 V ± 12 mV	S-1009N14I-M5T1U	S-1009N14I-N4T1U	S-1009N14I-I4T1U
1.5 V ± 12 mV	S-1009N15I-M5T1U	S-1009N15I-N4T1U	S-1009N15I-I4T1U
1.6 V ± 12 mV	S-1009N16I-M5T1U	S-1009N16I-N4T1U	S-1009N16I-I4T1U
1.7 V ± 12 mV	S-1009N17I-M5T1U	S-1009N17I-N4T1U	S-1009N17I-I4T1U
1.8 V ± 12 mV	S-1009N18I-M5T1U	S-1009N18I-N4T1U	S-1009N18I-I4T1U
1.9 V ± 12 mV	S-1009N19I-M5T1U	S-1009N19I-N4T1U	S-1009N19I-I4T1U
2.0 V ± 12 mV	S-1009N20I-M5T1U	S-1009N20I-N4T1U	S-1009N20I-I4T1U
2.1 V ± 12 mV	S-1009N21I-M5T1U	S-1009N21I-N4T1U	S-1009N21I-I4T1U
2.2 V ± 12 mV	S-1009N22I-M5T1U	S-1009N22I-N4T1U	S-1009N22I-I4T1U
2.3 V ± 12 mV	S-1009N23I-M5T1U	S-1009N23I-N4T1U	S-1009N23I-I4T1U
2.4 V ± 0.5%	S-1009N24I-M5T1U	S-1009N24I-N4T1U	S-1009N24I-I4T1U
2.5 V ± 0.5%	S-1009N25I-M5T1U	S-1009N25I-N4T1U	S-1009N25I-I4T1U
2.6 V ± 0.5%	S-1009N26I-M5T1U	S-1009N26I-N4T1U	S-1009N26I-I4T1U
2.7 V ± 0.5%	S-1009N27I-M5T1U	S-1009N27I-N4T1U	S-1009N27I-I4T1U
2.8 V ± 0.5%	S-1009N28I-M5T1U	S-1009N28I-N4T1U	S-1009N28I-I4T1U
2.9 V ± 0.5%	S-1009N29I-M5T1U	S-1009N29I-N4T1U	S-1009N29I-I4T1U
3.0 V ± 0.5%	S-1009N30I-M5T1U	S-1009N30I-N4T1U	S-1009N30I-I4T1U
3.1 V ± 0.5%	S-1009N31I-M5T1U	S-1009N31I-N4T1U	S-1009N31I-I4T1U
3.2 V ± 0.5%	S-1009N32I-M5T1U	S-1009N32I-N4T1U	S-1009N32I-I4T1U
3.3 V ± 0.5%	S-1009N33I-M5T1U	S-1009N33I-N4T1U	S-1009N33I-I4T1U
3.4 V ± 0.5%	S-1009N34I-M5T1U	S-1009N34I-N4T1U	S-1009N34I-I4T1U
3.5 V ± 0.5%	S-1009N35I-M5T1U	S-1009N35I-N4T1U	S-1009N35I-I4T1U
3.6 V ± 0.5%	S-1009N36I-M5T1U	S-1009N36I-N4T1U	S-1009N36I-I4T1U
3.7 V ± 0.5%	S-1009N37I-M5T1U	S-1009N37I-N4T1U	S-1009N37I-I4T1U
3.8 V ± 0.5%	S-1009N38I-M5T1U	S-1009N38I-N4T1U	S-1009N38I-I4T1U
3.9 V ± 0.5%	S-1009N39I-M5T1U	S-1009N39I-N4T1U	S-1009N39I-I4T1U
4.0 V ± 0.5%	S-1009N40I-M5T1U	S-1009N40I-N4T1U	S-1009N40I-I4T1U
4.1 V ± 0.5%	S-1009N41I-M5T1U	S-1009N41I-N4T1U	S-1009N41I-I4T1U
4.2 V ± 0.5%	S-1009N42I-M5T1U	S-1009N42I-N4T1U	S-1009N42I-I4T1U
4.3 V ± 0.5%	S-1009N43I-M5T1U	S-1009N43I-N4T1U	S-1009N43I-I4T1U
4.4 V ± 0.5%	S-1009N44I-M5T1U	S-1009N44I-N4T1U	S-1009N44I-I4T1U
4.5 V ± 0.5%	S-1009N45I-M5T1U	S-1009N45I-N4T1U	S-1009N45I-I4T1U
4.6 V ± 0.5%	S-1009N46I-M5T1U	S-1009N46I-N4T1U	S-1009N46I-I4T1U

3. 2 CMOS output product

Table 3

Detection Voltage	SOT-23-5	SC-82AB	SNT-4A
0.8 V ± 12 mV	S-1009C08I-M5T1U	S-1009C08I-N4T1U	S-1009C08I-I4T1U
0.9 V ± 12 mV	S-1009C09I-M5T1U	S-1009C09I-N4T1U	S-1009C09I-I4T1U
1.0 V ± 12 mV	S-1009C10I-M5T1U	S-1009C10I-N4T1U	S-1009C10I-I4T1U
1.1 V ± 12 mV	S-1009C11I-M5T1U	S-1009C11I-N4T1U	S-1009C11I-I4T1U
1.2 V ± 12 mV	S-1009C12I-M5T1U	S-1009C12I-N4T1U	S-1009C12I-I4T1U
1.3 V ± 12 mV	S-1009C13I-M5T1U	S-1009C13I-N4T1U	S-1009C13I-I4T1U
1.4 V ± 12 mV	S-1009C14I-M5T1U	S-1009C14I-N4T1U	S-1009C14I-I4T1U
1.5 V ± 12 mV	S-1009C15I-M5T1U	S-1009C15I-N4T1U	S-1009C15I-I4T1U
1.6 V ± 12 mV	S-1009C16I-M5T1U	S-1009C16I-N4T1U	S-1009C16I-I4T1U
1.7 V ± 12 mV	S-1009C17I-M5T1U	S-1009C17I-N4T1U	S-1009C17I-I4T1U
1.8 V ± 12 mV	S-1009C18I-M5T1U	S-1009C18I-N4T1U	S-1009C18I-I4T1U
1.9 V ± 12 mV	S-1009C19I-M5T1U	S-1009C19I-N4T1U	S-1009C19I-I4T1U
2.0 V ± 12 mV	S-1009C20I-M5T1U	S-1009C20I-N4T1U	S-1009C20I-I4T1U
2.1 V ± 12 mV	S-1009C21I-M5T1U	S-1009C21I-N4T1U	S-1009C21I-I4T1U
2.2 V ± 12 mV	S-1009C22I-M5T1U	S-1009C22I-N4T1U	S-1009C22I-I4T1U
2.3 V ± 12 mV	S-1009C23I-M5T1U	S-1009C23I-N4T1U	S-1009C23I-I4T1U
2.4 V ± 0.5%	S-1009C24I-M5T1U	S-1009C24I-N4T1U	S-1009C24I-I4T1U
2.5 V ± 0.5%	S-1009C25I-M5T1U	S-1009C25I-N4T1U	S-1009C25I-I4T1U
2.6 V ± 0.5%	S-1009C26I-M5T1U	S-1009C26I-N4T1U	S-1009C26I-I4T1U
2.7 V ± 0.5%	S-1009C27I-M5T1U	S-1009C27I-N4T1U	S-1009C27I-I4T1U
2.8 V ± 0.5%	S-1009C28I-M5T1U	S-1009C28I-N4T1U	S-1009C28I-I4T1U
2.9 V ± 0.5%	S-1009C29I-M5T1U	S-1009C29I-N4T1U	S-1009C29I-I4T1U
3.0 V ± 0.5%	S-1009C30I-M5T1U	S-1009C30I-N4T1U	S-1009C30I-I4T1U
3.1 V ± 0.5%	S-1009C31I-M5T1U	S-1009C31I-N4T1U	S-1009C31I-I4T1U
3.2 V ± 0.5%	S-1009C32I-M5T1U	S-1009C32I-N4T1U	S-1009C32I-I4T1U
3.3 V ± 0.5%	S-1009C33I-M5T1U	S-1009C33I-N4T1U	S-1009C33I-I4T1U
3.4 V ± 0.5%	S-1009C34I-M5T1U	S-1009C34I-N4T1U	S-1009C34I-I4T1U
3.5 V ± 0.5%	S-1009C35I-M5T1U	S-1009C35I-N4T1U	S-1009C35I-I4T1U
3.6 V ± 0.5%	S-1009C36I-M5T1U	S-1009C36I-N4T1U	S-1009C36I-I4T1U
3.7 V ± 0.5%	S-1009C37I-M5T1U	S-1009C37I-N4T1U	S-1009C37I-I4T1U
3.8 V ± 0.5%	S-1009C38I-M5T1U	S-1009C38I-N4T1U	S-1009C38I-I4T1U
3.9 V ± 0.5%	S-1009C39I-M5T1U	S-1009C39I-N4T1U	S-1009C39I-I4T1U
4.0 V ± 0.5%	S-1009C40I-M5T1U	S-1009C40I-N4T1U	S-1009C40I-I4T1U
4.1 V ± 0.5%	S-1009C41I-M5T1U	S-1009C41I-N4T1U	S-1009C41I-I4T1U
4.2 V ± 0.5%	S-1009C42I-M5T1U	S-1009C42I-N4T1U	S-1009C42I-I4T1U
4.3 V ± 0.5%	S-1009C43I-M5T1U	S-1009C43I-N4T1U	S-1009C43I-I4T1U
4.4 V ± 0.5%	S-1009C44I-M5T1U	S-1009C44I-N4T1U	S-1009C44I-I4T1U
4.5 V ± 0.5%	S-1009C45I-M5T1U	S-1009C45I-N4T1U	S-1009C45I-I4T1U
4.6 V ± 0.5%	S-1009C46I-M5T1U	S-1009C46I-N4T1U	S-1009C46I-I4T1U

■ Pin Configurations

1. SOT-23-5

Top view

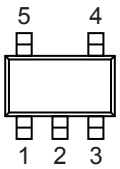


Figure 3

Table 4

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Input voltage pin
3	VSS	GND pin
4	NC*1	No connection
5	CD	Connection pin for delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

2. SC-82AB

Top view

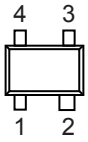


Figure 4

Table 5

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Input voltage pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

3. SNT-4A

Top view

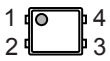


Figure 5

Table 6

Pin No.	Symbol	Description
1	VSS	GND pin
2	OUT	Voltage detection output pin
3	CD	Connection pin for delay capacitor
4	VDD	Input voltage pin

■ Absolute Maximum Ratings

Table 7

(Ta = +25°C unless otherwise specified)

Item			Symbol	Absolute Maximum Rating	Unit
Power supply voltage			$V_{DD} - V_{SS}$	12	V
CD pin input voltage			V_{CD}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output voltage	Nch open-drain output product		V_{OUT}	$V_{SS} - 0.3$ to 12.0	V
	CMOS output product			$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output current			I_{OUT}	50	mA
Power dissipation		SOT-23-5	P_D	600[*1]	mW
		SC-82AB		350[*1]	mW
		SNT-4A		300[*1]	mW
Operation ambient temperature			T_{opr}	−40 to +85	°C
Storage temperature			T_{stg}	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

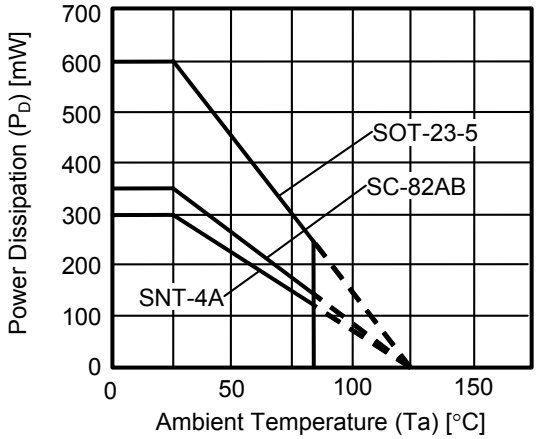


Figure 6 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Nch open-drain output product

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	0.8 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)}$ − 0.012	$-V_{DET(S)}$	$-V_{DET(S)}$ + 0.012	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)}$ × 0.995	$-V_{DET(S)}$	$-V_{DET(S)}$ × 1.005	V	1
Hysteresis width	V_{HYS}	−		$-V_{DET}$ × 0.04	$-V_{DET}$ × 0.05	$-V_{DET}$ × 0.06	V	1
Current consumption	I_{SS}	V_{DD} = +V_{DET} + 0.6 V	0.8 V ≤ $-V_{DET}$ < 1.2 V	−	0.30	0.90	μA	2
			1.2 V ≤ $-V_{DET}$ < 2.3 V	−	0.27	0.90	μA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	−	0.42	0.90	μA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	−	0.39	0.90	μA	2
Operation voltage	V_{DD}	−		0.7	−	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-1009N08 to 14	0.14	0.40	−	mA	3
			V_{DD} = 1.2 V S-1009N15 to 46	0.73	1.33	−	mA	3
			V_{DD} = 2.4 V S-1009N27 to 46	1.47	2.39	−	mA	3
Leakage current	I_{LEAK}	Output transistor Nch V_{DD} = 10.0 V, V_{OUT} = 10.0 V		−	−	0.08	μA	3
Delay time	t_D	C_D = 4.7 nF		22.1	26.0	29.9	ms	4
Detection voltage temperature coefficient*3	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40°C to +85°C	0.8 V ≤ $-V_{DET}$ < 0.9 V	−	±180	±430	ppm/°C	1
			0.9 V ≤ $-V_{DET}$ < 1.2 V	−	±120	±370	ppm/°C	1
			1.2 V ≤ $-V_{DET}$ ≤ 4.6 V	−	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 2**.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

***3.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}\ [mV/°C]^{*1} = -V_{DET(S)}\,(typ.)[V]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [ppm/°C]^{*3} \div 1000$$

- ***1.** Temperature change of the detection voltage
- ***2.** Set detection voltage
- ***3.** Detection voltage temperature coefficient

2. CMOS output product

Table 9

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	0.8 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.995$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.005$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.04$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.06$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	0.8 V ≤ $-V_{DET}$ < 1.2 V	–	0.30	0.90	μA	2
			1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	0.90	μA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	0.90	μA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	0.90	μA	2
Operation voltage	V_{DD}	–		0.6	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-1009C08 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-1009C15 to 46	0.73	1.33	–	mA	3
			V_{DD} = 2.4 V S-1009C27 to 46	1.47	2.39	–	mA	3
		Output transistor Pch V_{DS}*2 = 0.5 V	V_{DD} = 4.8 V S-1009C08 to 39	1.62	2.60	–	mA	5
			V_{DD} = 6.0 V S-1009C40 to 46	1.78	2.86	–	mA	5
Delay time	t_D	C_D = 4.7 nF		22.1	26.0	29.9	ms	4
Detection voltage temperature coefficient*3	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40°C to +85°C	0.8 V ≤ $-V_{DET}$ < 0.9 V	–	±180	±430	ppm/°C	1
			0.9 V ≤ $-V_{DET}$ < 1.2 V	–	±120	±370	ppm/°C	1
			1.2 V ≤ $-V_{DET}$ ≤ 4.6 V	–	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 3**.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

***3.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

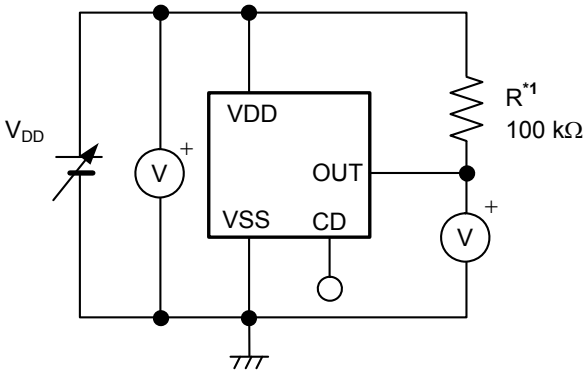
$$\frac{\Delta - V_{DET}}{\Delta Ta} \text{ [mV/°C]}^{*1} = -V_{DET(S)} \text{ (typ.)[V]}^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} \text{ [ppm/°C]}^{*3} \div 1000$$

***1.** Temperature change of the detection voltage

***2.** Set detection voltage

***3.** Detection voltage temperature coefficient

■ Test Circuits



***1.** R is unnecessary for CMOS output product.

Figure 7 Test Circuit 1

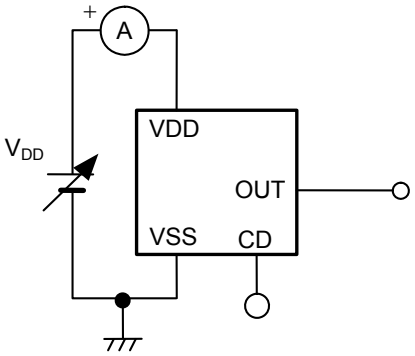


Figure 8 Test Circuit 2

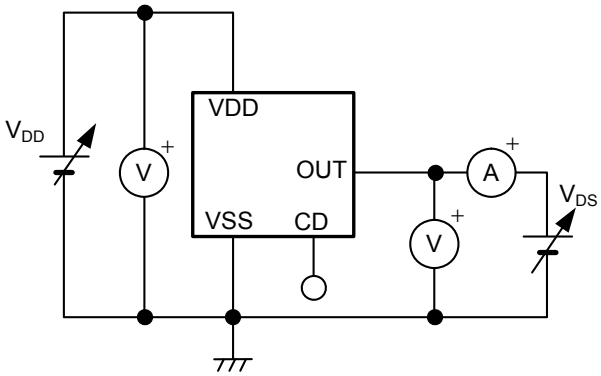
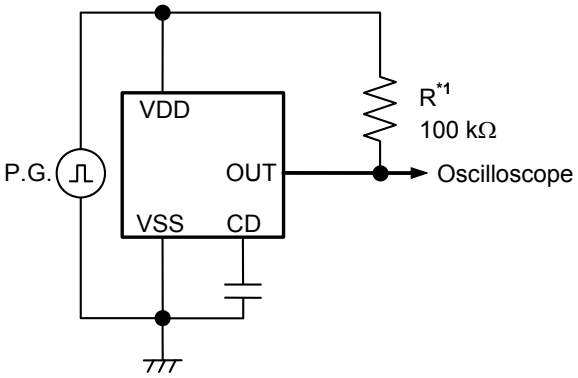


Figure 9 Test Circuit 3



***1.** R is unnecessary for CMOS output product.

Figure 10 Test Circuit 4

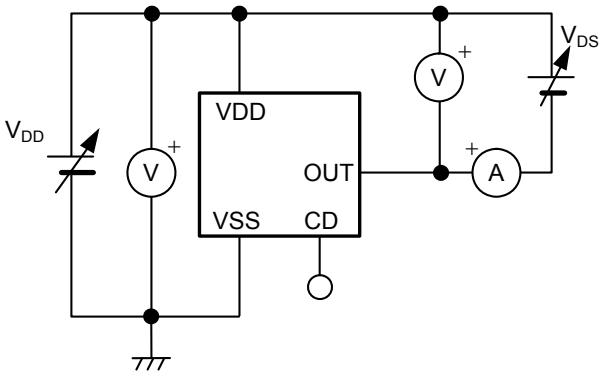


Figure 11 Test Circuit 5

■ Timing Charts

1. Nch open-drain output product

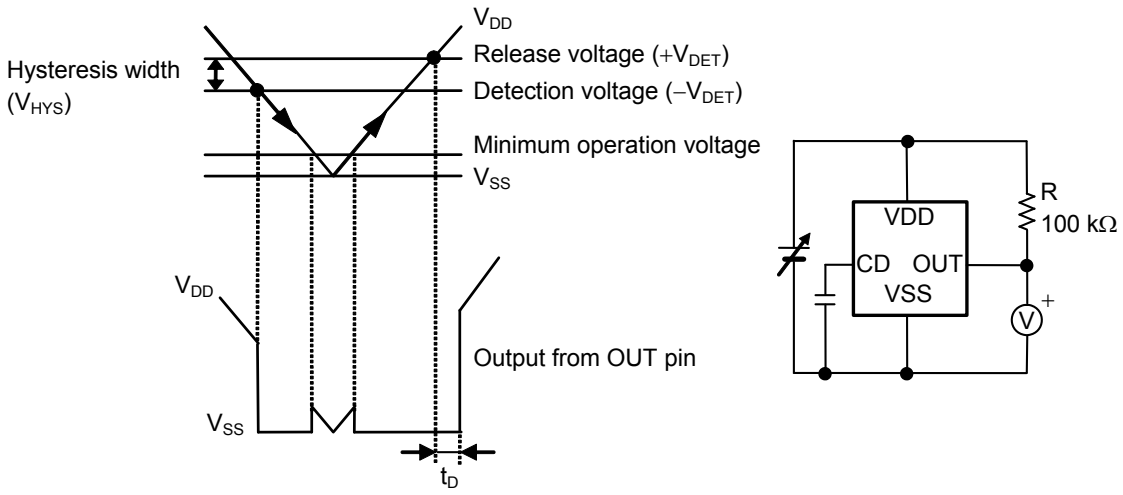
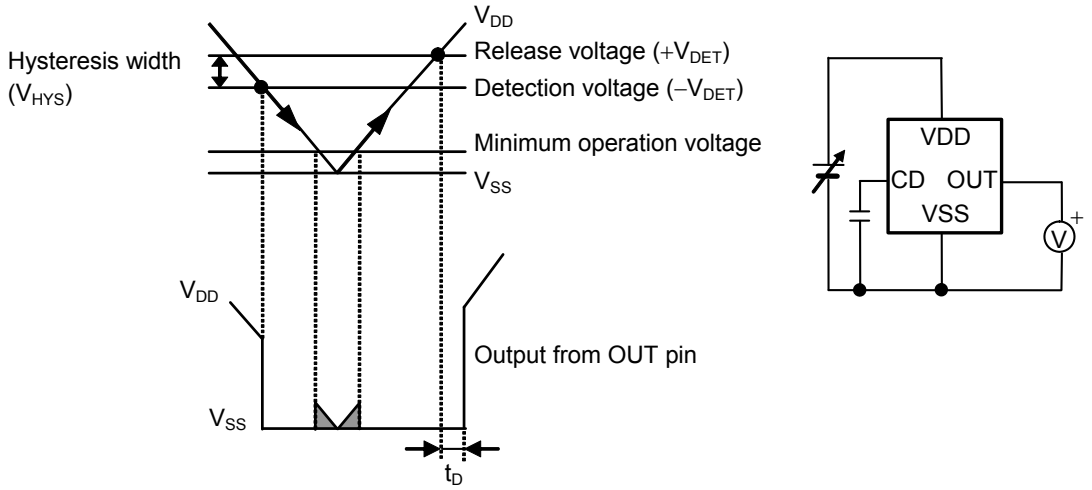


Figure 12

2. CMOS output product



Remark When V_{DD} is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.

Figure 13

■ Operation

1. Basic operation: CMOS output (active "L") product

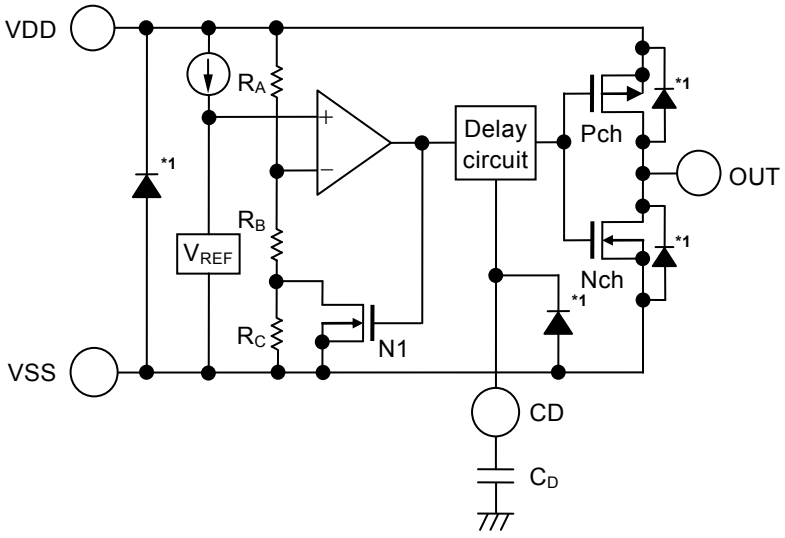
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or more, the Nch transistor is OFF and the Pch transistor is ON to output V_{DD} ("H"). Since the Nch transistor N1 in **Figure 14** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) Although V_{DD} decreases to $+V_{DET}$ or less, V_{DD} is output when V_{DD} is the detection voltage ($-V_{DET}$) or more. When V_{DD} decreases to $-V_{DET}$ or less (point A in **Figure 15**), the Nch transistor is ON and the Pch transistor is OFF so that V_{SS} is output. At this time, the Nch transistor N1 in **Figure 14** is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is indefinite by decreasing V_{DD} to the IC's minimum operation voltage or less. If the output is pulled up, it will be V_{DD}.

(4) V_{SS} is output by increasing V_{DD} to the minimum operation voltage or more. Although V_{DD} exceeds $-V_{DET}$ and V_{DD} is less than $+V_{DET}$, the output is V_{SS}.

(5) When increasing V_{DD} to $+V_{DET}$ or more (point B in **Figure 15**), the Nch transistor is OFF and the Pch transistor is ON so that V_{DD} is output. At this time, V_{DD} is output from the OUT pin after the passage of the delay time (t_D).



***1.** Parasiteic diode

Figure 14 Operation 1

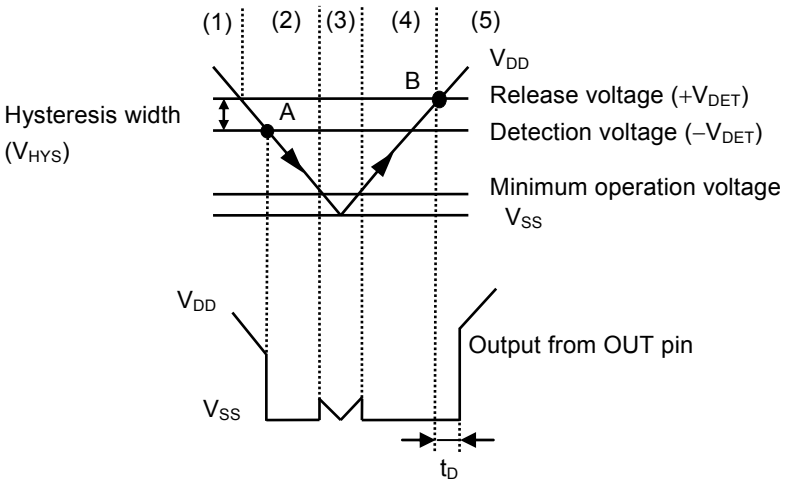


Figure 15 Operation 2

2. Delay circuit

The delay circuit delays the output signal to the OUT pin from the time at which the power supply voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when V_{DD} decreases to the detection voltage ($-V_{DET}$) or less (refer to "**Figure 15 Operation 2**").
The delay time (t_D) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached delay capacitor (C_D), or the delay time (t_{D0}) when the CD pin is open, and calculated from the following equation. When the C_D value is sufficiently large, the t_{D0} value can be disregarded.

t_D [ms] = Delay coefficient $\times$ C_D [nF] + t_{D0} [ms]

Table 10 Delay Coefficient

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +85°C	2.82	4.20	5.72
Ta = +25°C	4.70	5.47	6.24
Ta = −40°C	5.64	8.40	12.01

Table 11 Delay Time

Operation Temperature	Delay Time (t_{D0})		
	Min.	Typ.	Max.
Ta = −40°C to +85°C	0.01 ms	0.10 ms	0.24 ms

Caution 1. When the CD pin is open, a double pulse shown in Figure 16 may appear at release. To avoid the double pulse, attach 100 pF or larger capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.

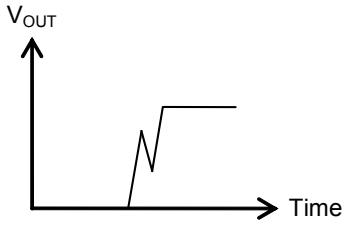


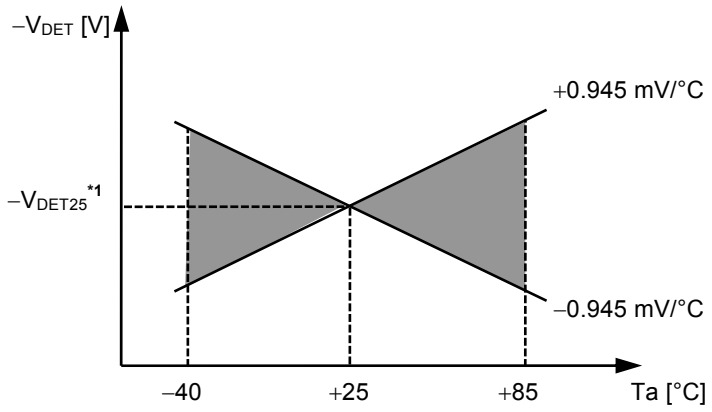
Figure 16

2. **Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.**
3. **There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.**

3. Other characteristics

3. 1 Temperature characteristics of detection voltage

The shaded area in **Figure 17** shows the temperature characteristics of detection voltage in the operation temperature range.



***1.** $-V_{DET25}$ is an actual detection voltage value at Ta = +25°C.

Figure 17 Temperature Characteristics of Detection Voltage (Example for $-V_{DET}$ = 2.7 V)

3. 2 Temperature characteristics of release voltage

The temperature change $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by using the temperature change $\frac{\Delta - V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

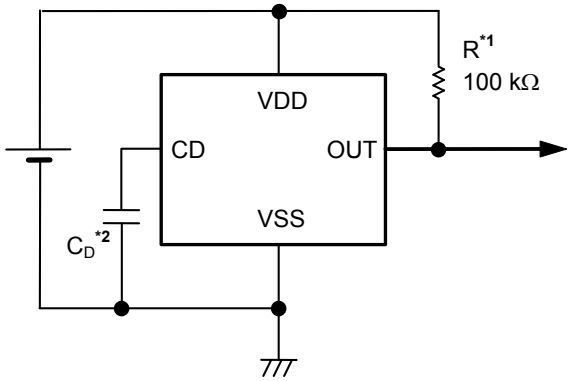
The temperature change of the release voltage and the detection voltage has the same sign consequently.

3. 3 Temperature characteristics of hysteresis voltage

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

■ Standard Circuit



***1.** R is unnecessary for CMOS output product.

***2.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 18

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 21** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (refer to **Figure 19**).

Example: In the S-1009C15, the detection voltage is either one in the range of 1.488 V ≤ $-V_{DET}$ ≤ 1.512 V.
This means that some S-1009C15 have $-V_{DET}$ = 1.488 V and some have $-V_{DET}$ = 1.512 V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 21** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (refer to **Figure 20**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.04 \leq +V_{DET} \leq -V_{DET} \times 1.06$.

Example: For the S-1009C15, the release voltage is either one in the range of 1.548 V ≤ $+V_{DET}$ ≤ 1.602 V.
This means that some S-1009C15 have $+V_{DET}$ = 1.548 V and some have $+V_{DET}$ = 1.602 V.

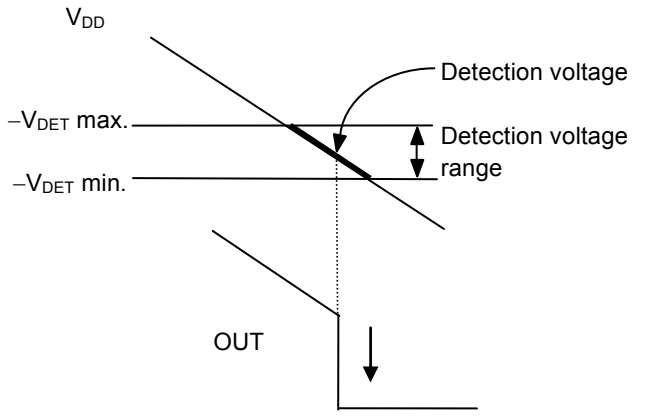


Figure 19 Detection Voltage

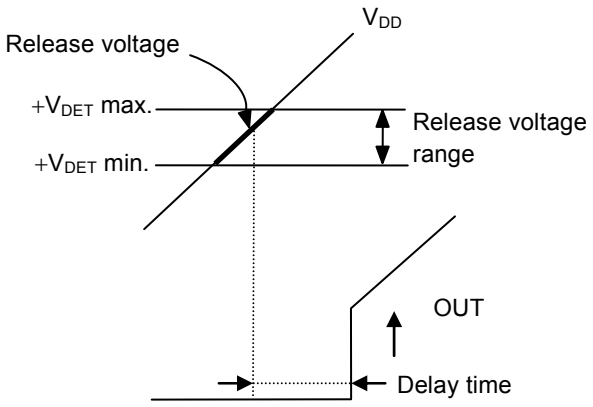
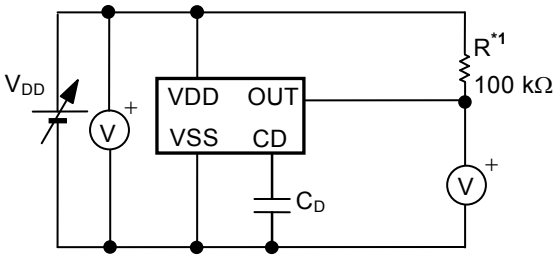


Figure 20 Release Voltage



***1.** R is unnecessary for CMOS output product.

Figure 21 Test Circuit of Detection Voltage and Release Voltage

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = V_{HYS} in "**Figure 15 Operation 2**"). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

4. Delay time (t_D)

The delay time in the S-1009 Series is a period from the input voltage to the VDD pin exceeding the release voltage ($+V_{DET}$) until the output from the OUT pin inverts. The delay time changes according to the delay capacitor (C_D).

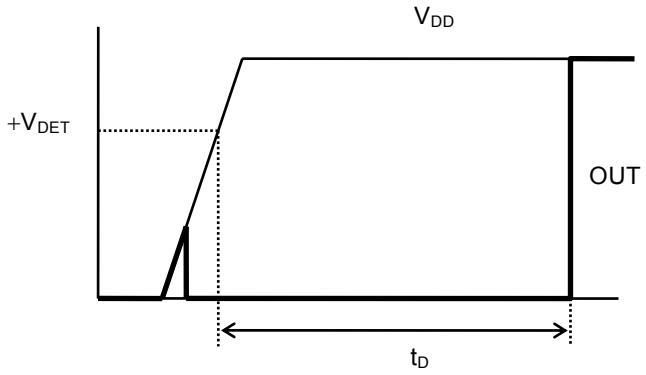


Figure 22 Delay Time

5. Feed-through current

Feed-through current is a current that flows instantaneously at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

6. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 23**), taking a CMOS active "L" product for example, the feed-through current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [feed-through current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

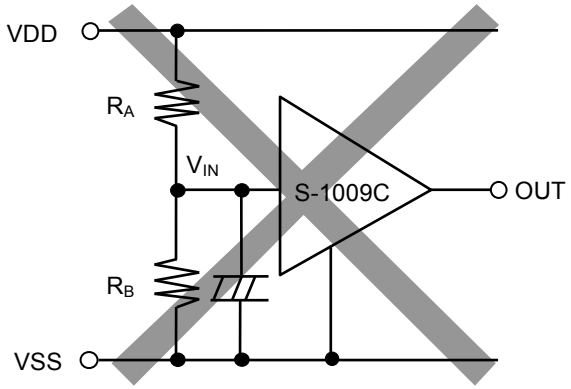


Figure 23 Example for Bad Implementation Due to Detection Voltage Change

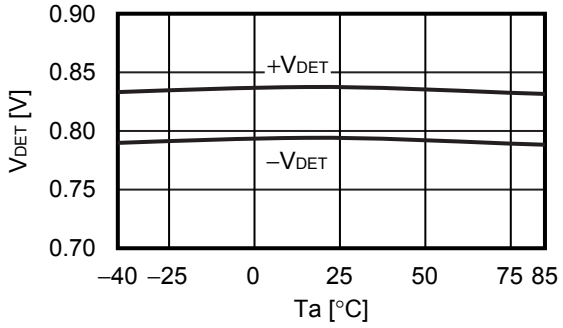
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product of the S-1009 Series, the feed-through current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the feed-through current during releasing.
- In CMOS output product oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

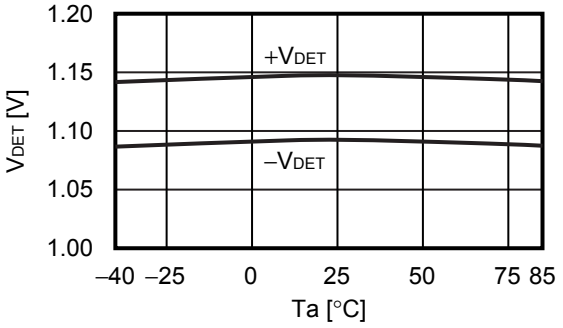
■ Characteristics (Typical Data)

1. Detection voltage (V_{DET}) vs. Temperature (Ta)

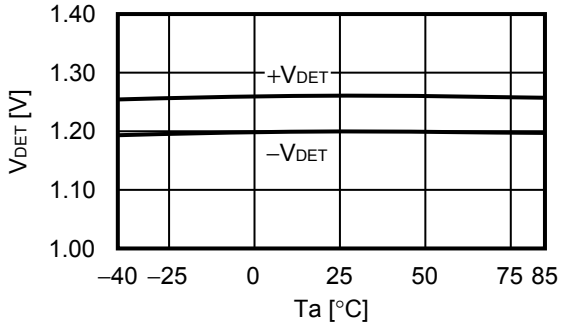
S-1009N08



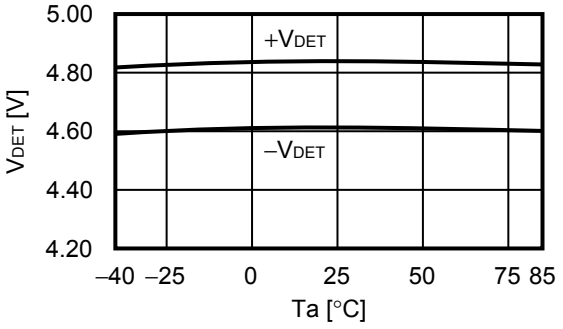
S-1009N11



S-1009N12

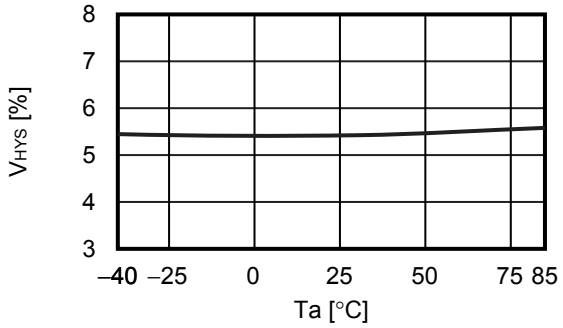


S-1009N46

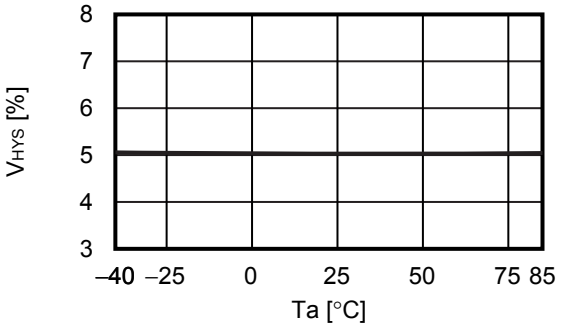


2. Hysteresis width (V_{HYS}) vs. Temperature (Ta)

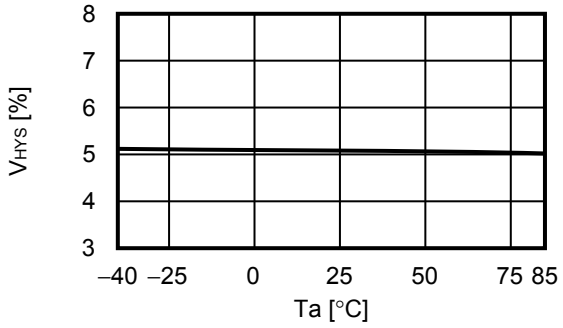
S-1009N08



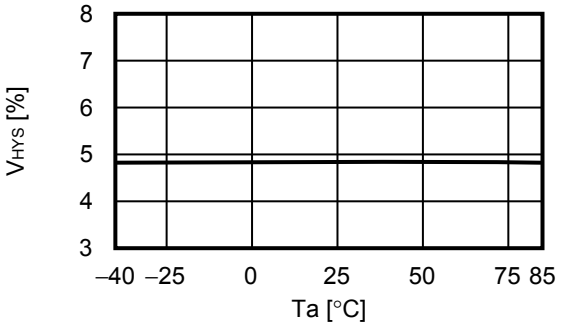
S-1009N11



S-1009N12

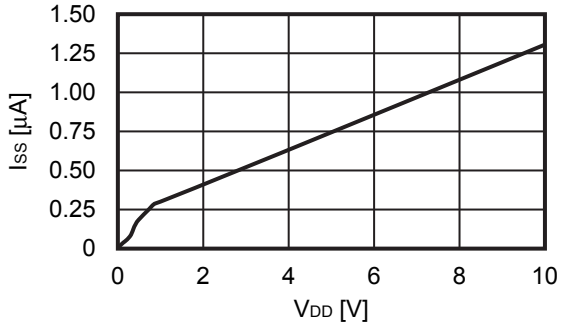


S-1009N46

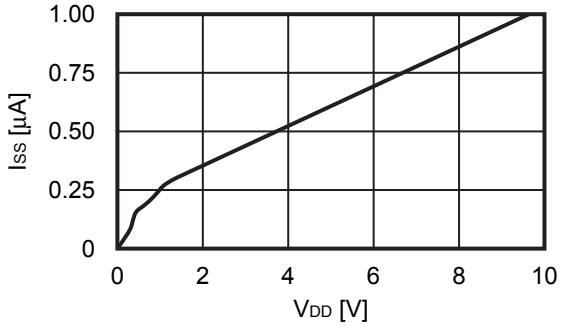


3. Current consumption (I_{SS}) vs. Input voltage (V_{DD})

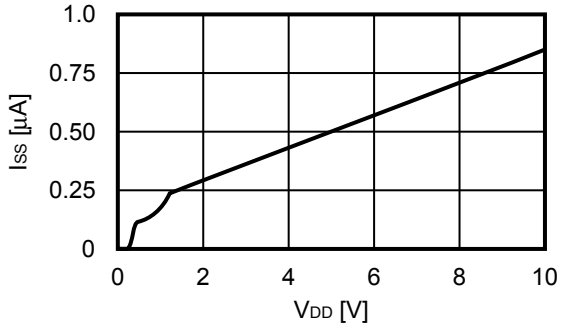
S-1009C08 Ta = +25°C



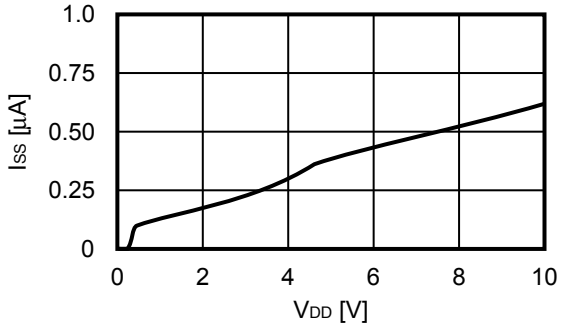
S-1009C11 Ta = +25°C



S-1009C12 Ta = +25°C

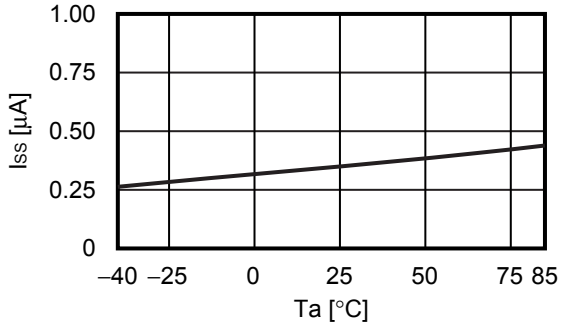


S-1009C46 Ta = +25°C

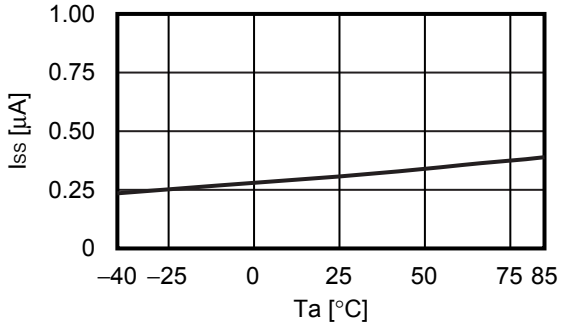


4. Current consumption (I_{SS}) vs. Temperature (Ta)

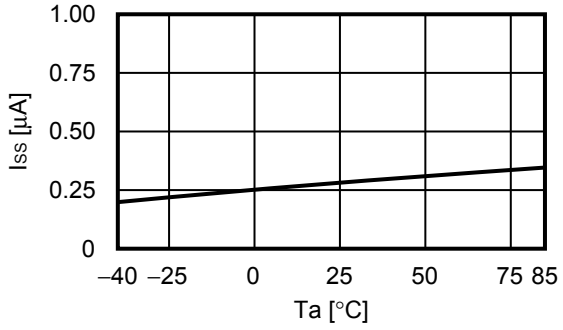
S-1009N08 V_{DD} = +V_{DET} + 0.6 V



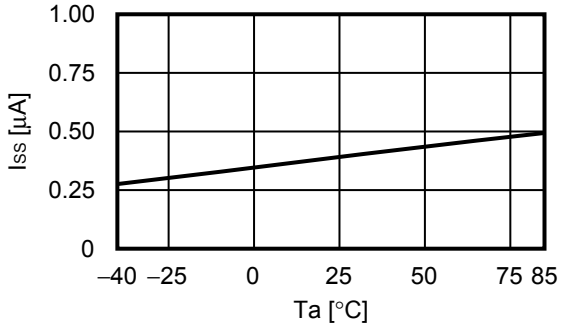
S-1009N11 V_{DD} = +V_{DET} + 0.6 V



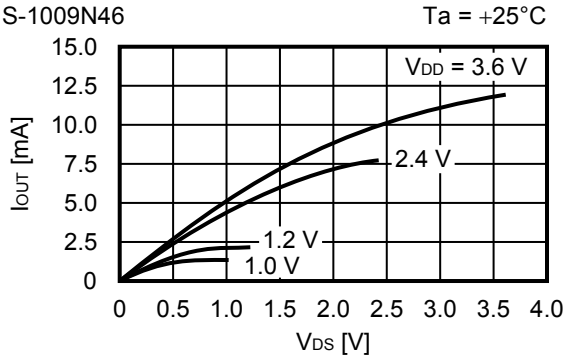
S-1009N12 V_{DD} = +V_{DET} + 0.6 V



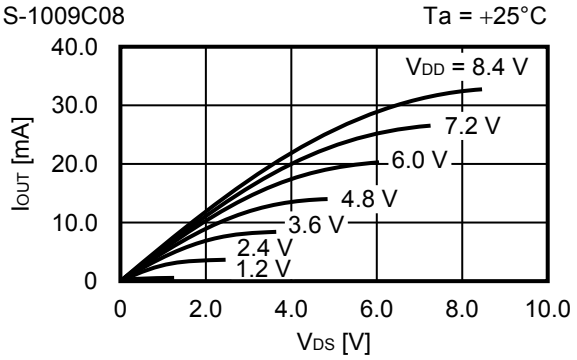
S-1009N46 V_{DD} = +V_{DET} + 0.6 V



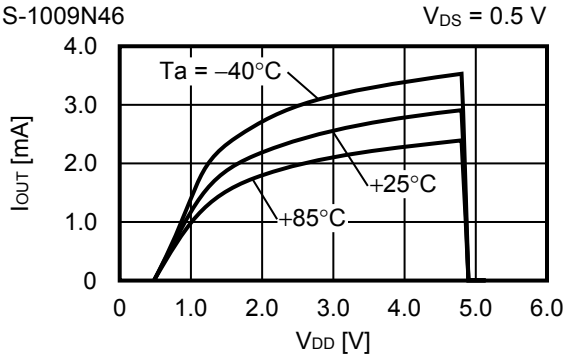
5. Nch transistor output current (I_{OUT}) vs. V_{DS}



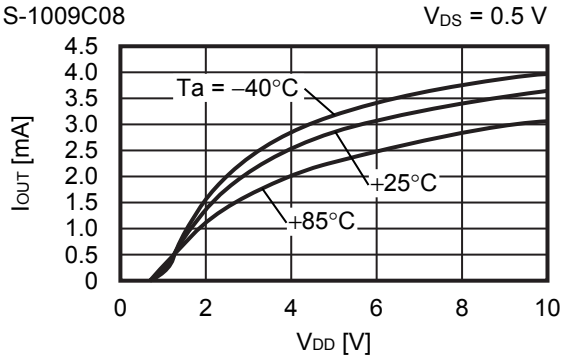
6. Pch transistor output current (I_{OUT}) vs. V_{DS}



7. Nch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})



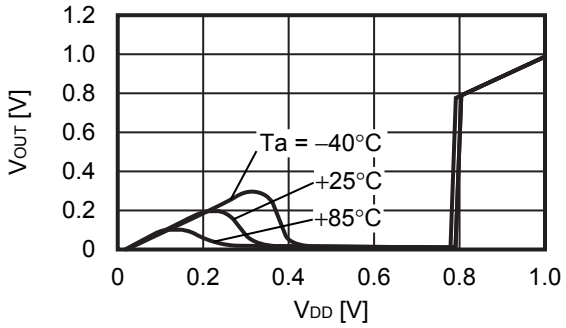
8. Pch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})



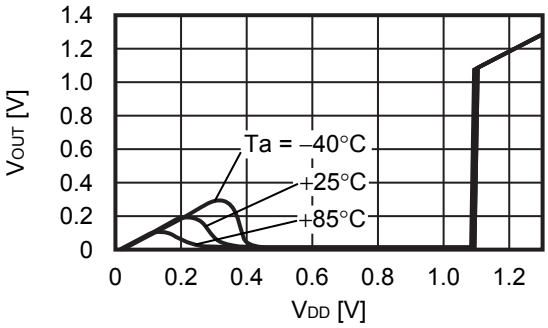
Remark V_{DS}: Drain-to-source voltage of the output transistor

9. Minimum operation voltage (V_{OUT}) vs. Input voltage (V_{DD})

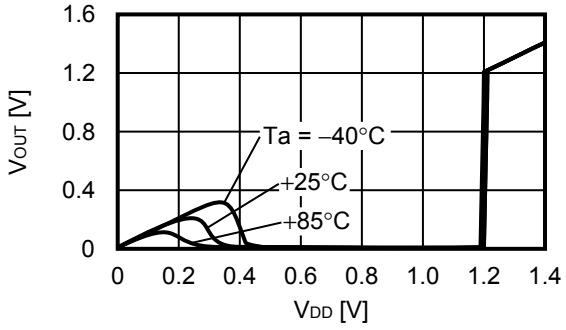
S-1009N08 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



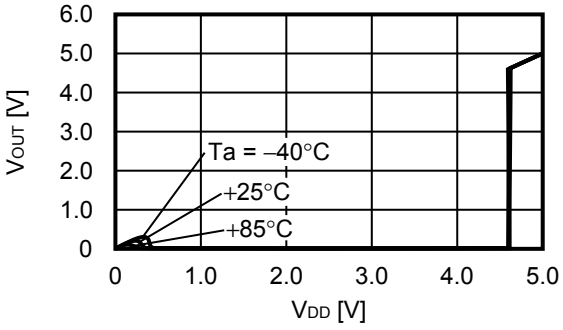
S-1009N11 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



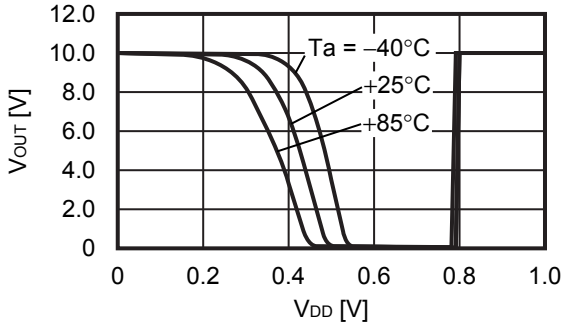
S-1009N12 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



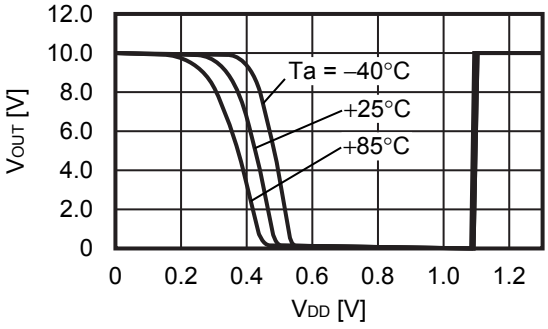
S-1009N46 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



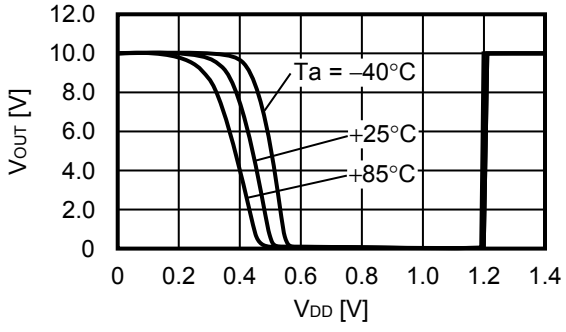
S-1009N08 Pull-up to 10 V
Pull-up resistance: 100 kΩ



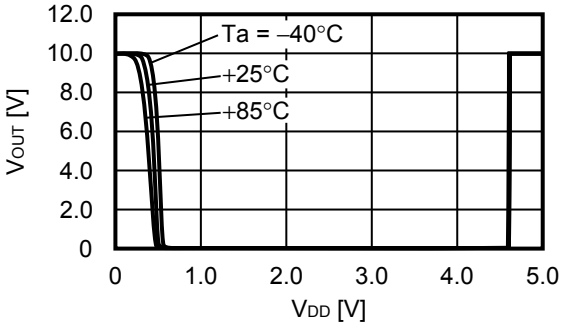
S-1009N11 Pull-up to 10 V
Pull-up resistance: 100 kΩ



S-1009N12 Pull-up to 10 V
Pull-up resistance: 100 kΩ

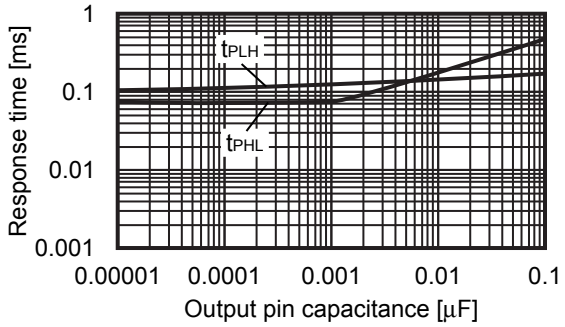


S-1009N46 Pull-up to 10 V
Pull-up resistance: 100 kΩ

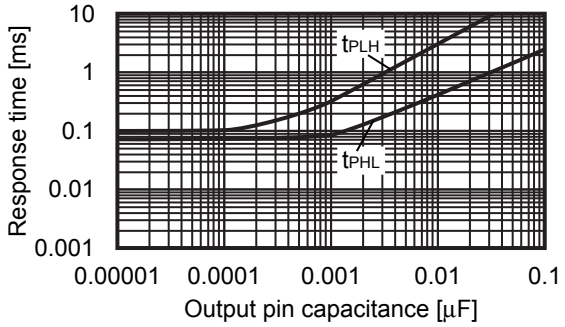


10. Dynamic response vs. Output pin capacitance (C_{OUT}) (CD pin; open)

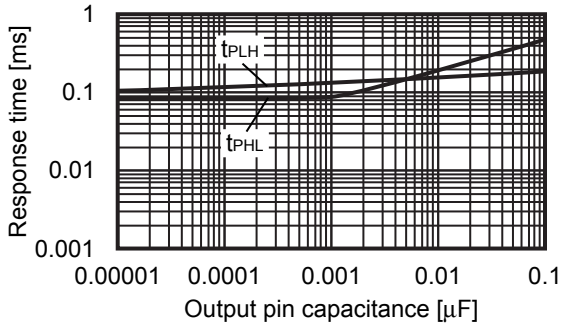
S-1009C08



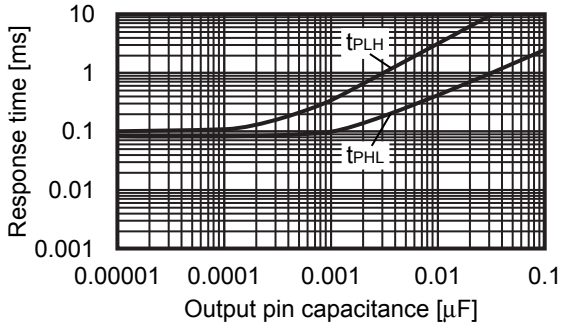
S-1009N08



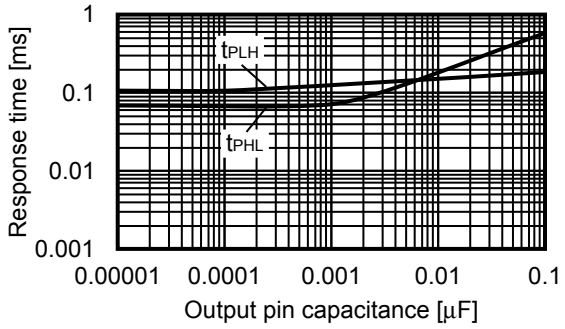
S-1009C11



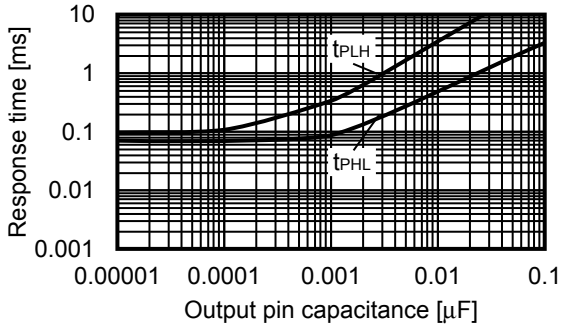
S-1009N11



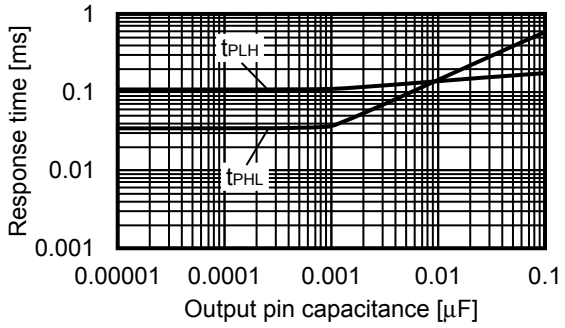
S-1009C12



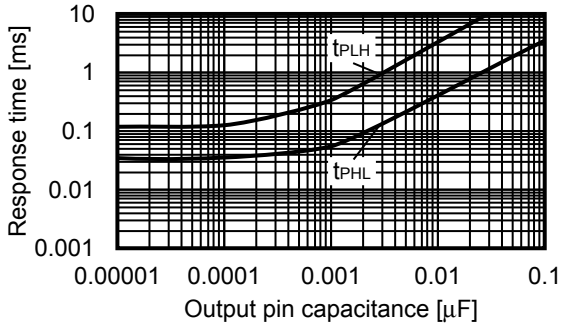
S-1009N12

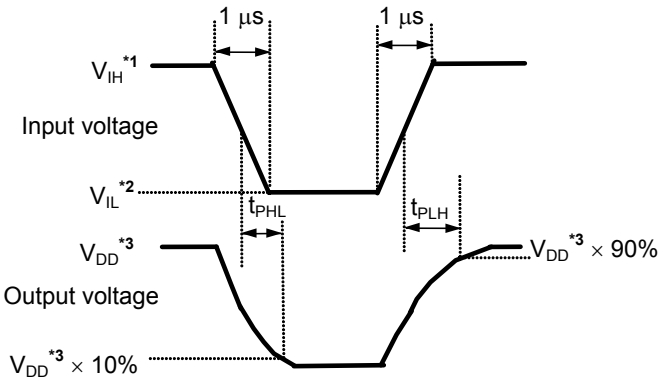


S-1009C46



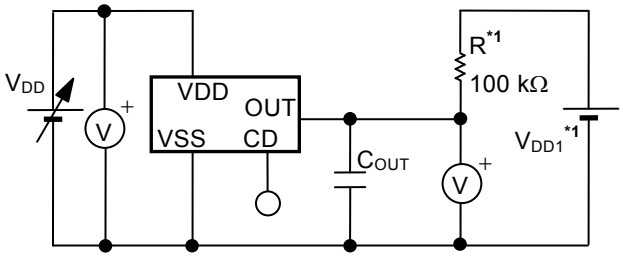
S-1009N46





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.7 V
***3.** CMOS output product: V_{DD}
Nch open-drain product: V_{DD1}

Figure 24 Test Condition of Response Time

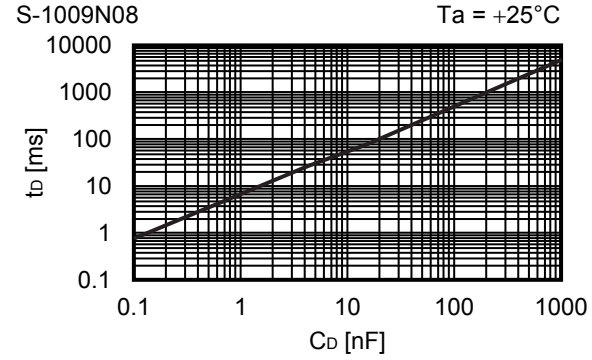


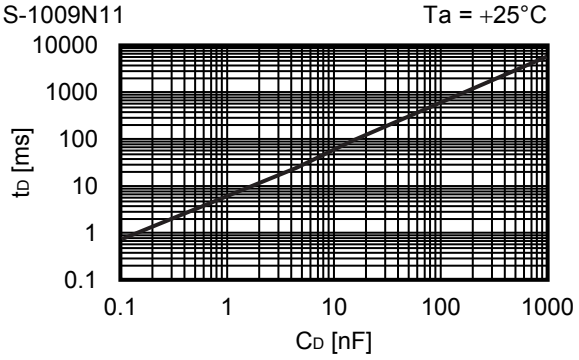
***1.** R and V_{DD1} are unnecessary for CMOS output product.

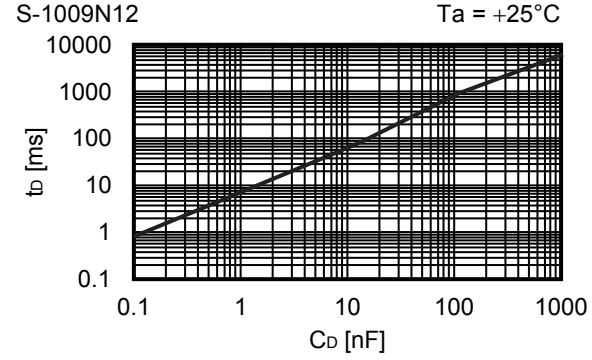
Figure 25 Test Circuit of Response Time

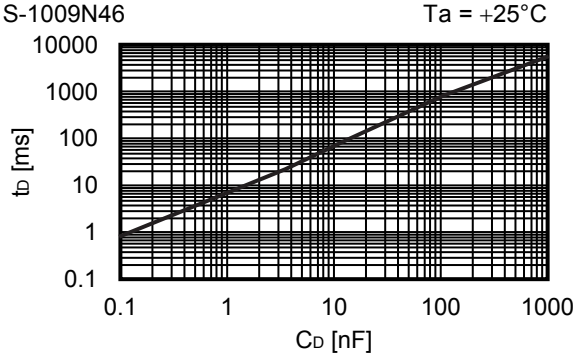
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. When the CD pin is open, a double pulse may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Response time when detecting (t_{PHL}) is not affected by CD pin capacitance. Besides, response time when releasing (t_{PLH}) can be set the delay time by attaching the CD pin. Refer to "11. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance)" for details.

11. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance)

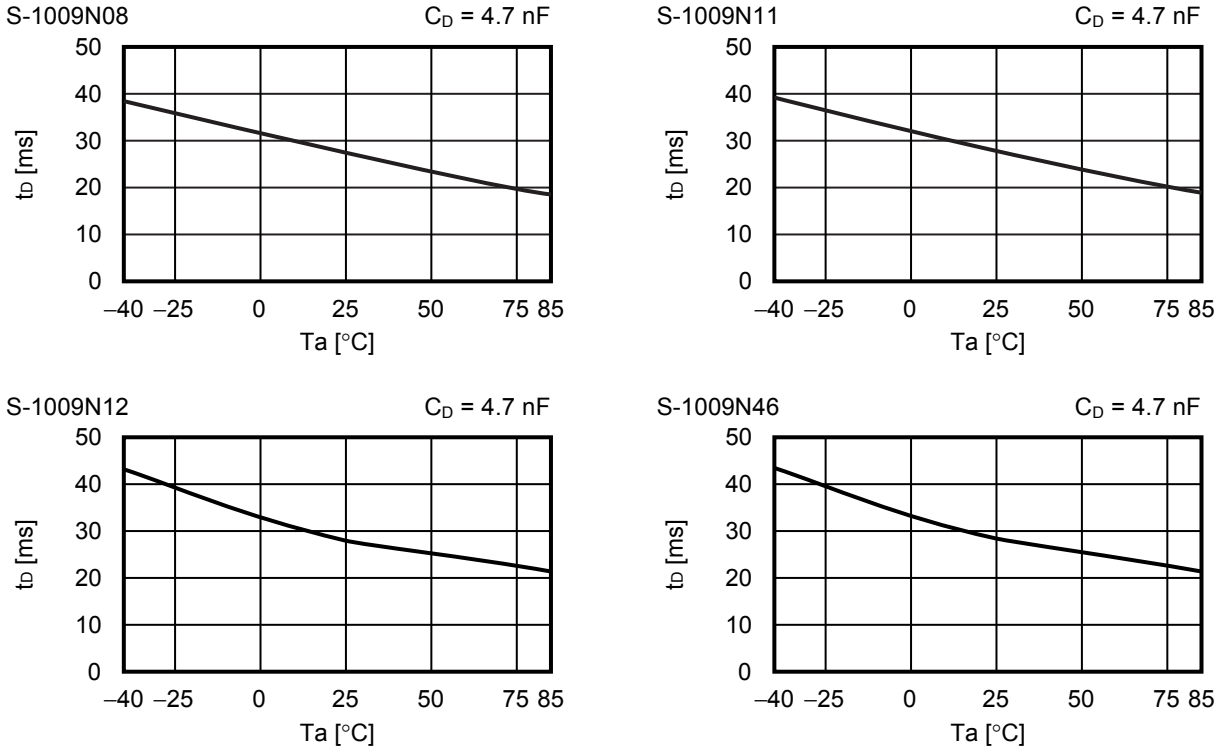


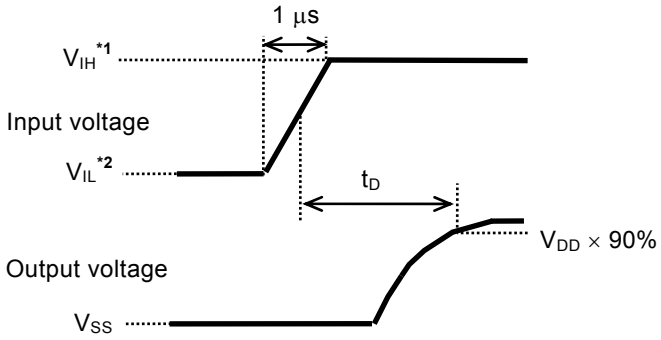






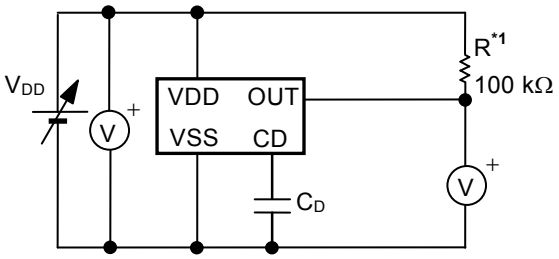
12. Delay time (t_D) vs. Temperature (Ta)





*1. V_{IH} = 10 V
*2. V_{IL} = 0.7 V

Figure 26 Test Condition for Delay Time



*1. R is unnecessary for CMOS output product.

Figure 27 Test Circuit for Delay Time

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the guaranteed operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.

Using the S-1009 Series which has the low operation voltage, a high accuracy detection voltage and hysteresis, reset circuits can be easily constructed as seen in **Figure 28** and **Figure 29**.

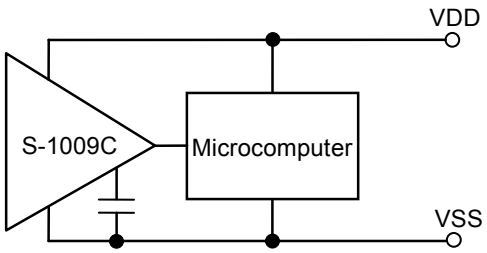


Figure 28 Example of Reset Circuit (CMOS Output Product)

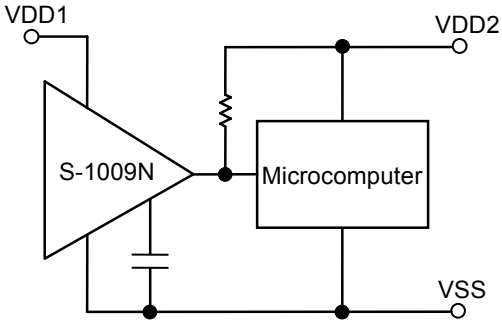
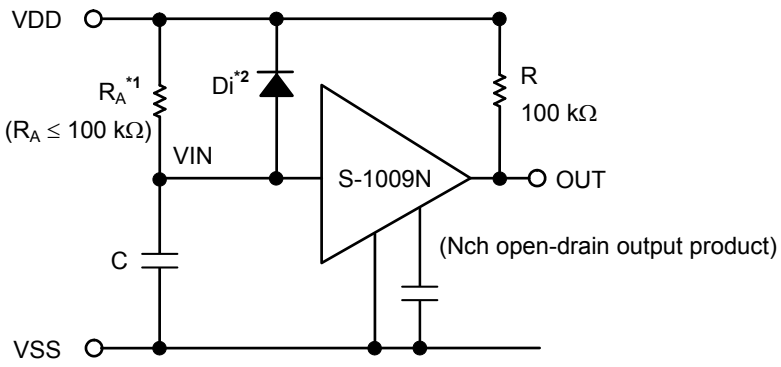


Figure 29 Example of Reset Circuit (Nch Open-drain Output Product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Power-on reset circuit (Nch open-drain output product only)

A power-on reset circuit can be constructed using the S-1009N Series.



***1.** R_A should be 100 kΩ or less to prevent oscillation.

***2.** Diode (Di) instantaneously discharges the charge stored in the capacitor (C) at the power falling. Di can be removed when the delay of the falling time is not important.

Figure 30

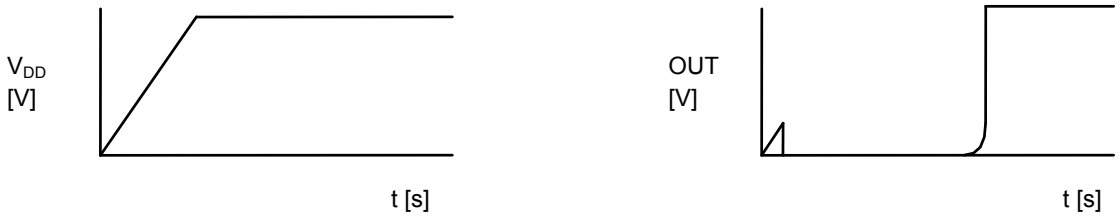


Figure 31

Remark When the power rises sharply, the output may instantaneously be set to the "H" level due to the IC's indefinite area (the output voltage is indefinite when it is the IC's minimum operation voltage or less), as seen in **Figure 32.**

Figure 32

Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Note that the hysteresis width may be larger as the following equation shows when using the above connection. Perform thorough evaluation using the actual application to set the constant.

Maximum hysteresis width = $V_{HYS} + R_A \bullet 20\ \mu A$

3. Change of detection voltage (Nch open-drain output product only)

If there is not a product with a specified detection voltage value in the S-1009N Series, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 33** and **Figure 34**.
In **Figure 33**, hysteresis width also changes.

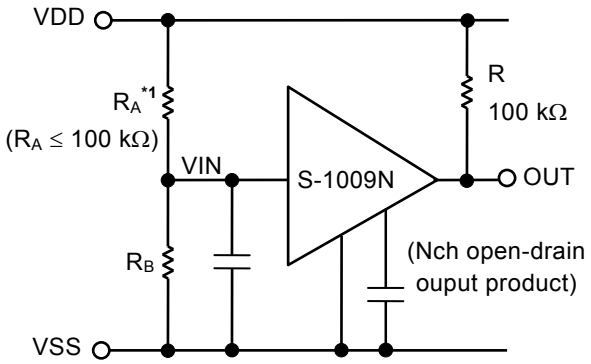


Figure 33

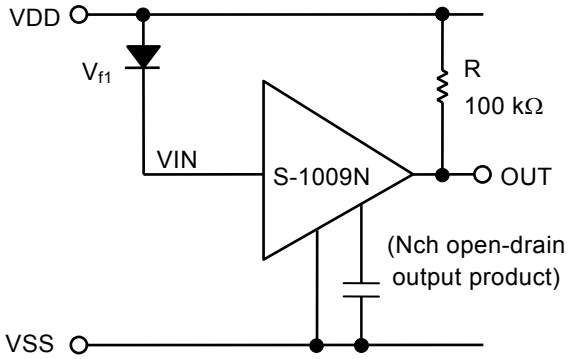


Figure 34

$$\text{Detection voltage} = \frac{R_A + R_B}{R_B} \bullet -V_{DET}$$

$$\text{Hysteresis width} = \frac{R_A + R_B}{R_B} \bullet V_{HYS}$$

$$\text{Detection voltage} = V_{f1} + (-V_{DET})$$

***1.** R_A should be 100 kΩ or less to prevent oscillation.

Caution If R_A and R_B are large, the hysteresis width may also be larger than the value given by the above equation due to the feed-through current.

Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

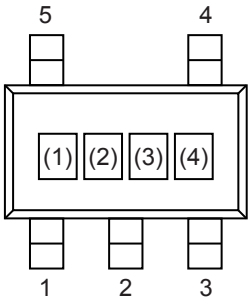
2. Note that the hysteresis width may be larger as the following equation shows when using the above connections. Perform thorough evaluation using the actual application to set the constant.

$$\textbf{Maximum hysteresis width} = \frac{R_A + R_B}{R_B} \bullet V_{HYS} + R_A \bullet 20\ \mu A$$

■ Marking Specifications

1. SOT-23-5

Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)
(4): Lot number

Product name vs. Product code

1. 1 Nch open-drain output product

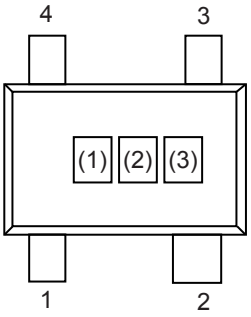
Product Name	Product Code		
	(1)	(2)	(3)
S-1009N08I-M5T1U	T	8	A
S-1009N09I-M5T1U	T	8	B
S-1009N10I-M5T1U	T	8	C
S-1009N11I-M5T1U	T	8	D
S-1009N12I-M5T1U	T	8	E
S-1009N13I-M5T1U	T	8	F
S-1009N14I-M5T1U	T	8	G
S-1009N15I-M5T1U	T	8	H
S-1009N16I-M5T1U	T	8	I
S-1009N17I-M5T1U	T	8	J
S-1009N18I-M5T1U	T	8	K
S-1009N19I-M5T1U	T	8	L
S-1009N20I-M5T1U	T	8	M
S-1009N21I-M5T1U	T	8	N
S-1009N22I-M5T1U	T	8	O
S-1009N23I-M5T1U	T	8	P
S-1009N24I-M5T1U	T	8	Q
S-1009N25I-M5T1U	T	8	R
S-1009N26I-M5T1U	T	8	S
S-1009N27I-M5T1U	T	8	T
S-1009N28I-M5T1U	T	8	U
S-1009N29I-M5T1U	T	8	V
S-1009N30I-M5T1U	T	8	W
S-1009N31I-M5T1U	T	8	X
S-1009N32I-M5T1U	T	8	Y
S-1009N33I-M5T1U	T	8	Z
S-1009N34I-M5T1U	T	9	A
S-1009N35I-M5T1U	T	9	B
S-1009N36I-M5T1U	T	9	C
S-1009N37I-M5T1U	T	9	D
S-1009N38I-M5T1U	T	9	E
S-1009N39I-M5T1U	T	9	F
S-1009N40I-M5T1U	T	9	G
S-1009N41I-M5T1U	T	9	H
S-1009N42I-M5T1U	T	9	I
S-1009N43I-M5T1U	T	9	J
S-1009N44I-M5T1U	T	9	K
S-1009N45I-M5T1U	T	9	L
S-1009N46I-M5T1U	T	9	M

1. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-1009C08I-M5T1U	T	6	A
S-1009C09I-M5T1U	T	6	B
S-1009C10I-M5T1U	T	6	C
S-1009C11I-M5T1U	T	6	D
S-1009C12I-M5T1U	T	6	E
S-1009C13I-M5T1U	T	6	F
S-1009C14I-M5T1U	T	6	G
S-1009C15I-M5T1U	T	6	H
S-1009C16I-M5T1U	T	6	I
S-1009C17I-M5T1U	T	6	J
S-1009C18I-M5T1U	T	6	K
S-1009C19I-M5T1U	T	6	L
S-1009C20I-M5T1U	T	6	M
S-1009C21I-M5T1U	T	6	N
S-1009C22I-M5T1U	T	6	O
S-1009C23I-M5T1U	T	6	P
S-1009C24I-M5T1U	T	6	Q
S-1009C25I-M5T1U	T	6	R
S-1009C26I-M5T1U	T	6	S
S-1009C27I-M5T1U	T	6	T
S-1009C28I-M5T1U	T	6	U
S-1009C29I-M5T1U	T	6	V
S-1009C30I-M5T1U	T	6	W
S-1009C31I-M5T1U	T	6	X
S-1009C32I-M5T1U	T	6	Y
S-1009C33I-M5T1U	T	6	Z
S-1009C34I-M5T1U	T	7	A
S-1009C35I-M5T1U	T	7	B
S-1009C36I-M5T1U	T	7	C
S-1009C37I-M5T1U	T	7	D
S-1009C38I-M5T1U	T	7	E
S-1009C39I-M5T1U	T	7	F
S-1009C40I-M5T1U	T	7	G
S-1009C41I-M5T1U	T	7	H
S-1009C42I-M5T1U	T	7	I
S-1009C43I-M5T1U	T	7	J
S-1009C44I-M5T1U	T	7	K
S-1009C45I-M5T1U	T	7	L
S-1009C46I-M5T1U	T	7	M

2. SC-82AB

Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)

Product name vs. Product code

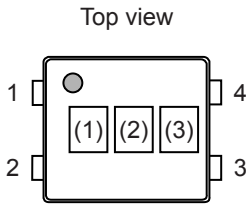
2. 1 Nch open-drain output product

Product Name	Product Code		
	(1)	(2)	(3)
S-1009N08I-N4T1U	T	8	A
S-1009N09I-N4T1U	T	8	B
S-1009N10I-N4T1U	T	8	C
S-1009N11I-N4T1U	T	8	D
S-1009N12I-N4T1U	T	8	E
S-1009N13I-N4T1U	T	8	F
S-1009N14I-N4T1U	T	8	G
S-1009N15I-N4T1U	T	8	H
S-1009N16I-N4T1U	T	8	I
S-1009N17I-N4T1U	T	8	J
S-1009N18I-N4T1U	T	8	K
S-1009N19I-N4T1U	T	8	L
S-1009N20I-N4T1U	T	8	M
S-1009N21I-N4T1U	T	8	N
S-1009N22I-N4T1U	T	8	O
S-1009N23I-N4T1U	T	8	P
S-1009N24I-N4T1U	T	8	Q
S-1009N25I-N4T1U	T	8	R
S-1009N26I-N4T1U	T	8	S
S-1009N27I-N4T1U	T	8	T
S-1009N28I-N4T1U	T	8	U
S-1009N29I-N4T1U	T	8	V
S-1009N30I-N4T1U	T	8	W
S-1009N31I-N4T1U	T	8	X
S-1009N32I-N4T1U	T	8	Y
S-1009N33I-N4T1U	T	8	Z
S-1009N34I-N4T1U	T	9	A
S-1009N35I-N4T1U	T	9	B
S-1009N36I-N4T1U	T	9	C
S-1009N37I-N4T1U	T	9	D
S-1009N38I-N4T1U	T	9	E
S-1009N39I-N4T1U	T	9	F
S-1009N40I-N4T1U	T	9	G
S-1009N41I-N4T1U	T	9	H
S-1009N42I-N4T1U	T	9	I
S-1009N43I-N4T1U	T	9	J
S-1009N44I-N4T1U	T	9	K
S-1009N45I-N4T1U	T	9	L
S-1009N46I-N4T1U	T	9	M

2. 2 CMOS output product

Product Name	Product Code		
	(1)	(2)	(3)
S-1009C08I-N4T1U	T	6	A
S-1009C09I-N4T1U	T	6	B
S-1009C10I-N4T1U	T	6	C
S-1009C11I-N4T1U	T	6	D
S-1009C12I-N4T1U	T	6	E
S-1009C13I-N4T1U	T	6	F
S-1009C14I-N4T1U	T	6	G
S-1009C15I-N4T1U	T	6	H
S-1009C16I-N4T1U	T	6	I
S-1009C17I-N4T1U	T	6	J
S-1009C18I-N4T1U	T	6	K
S-1009C19I-N4T1U	T	6	L
S-1009C20I-N4T1U	T	6	M
S-1009C21I-N4T1U	T	6	N
S-1009C22I-N4T1U	T	6	O
S-1009C23I-N4T1U	T	6	P
S-1009C24I-N4T1U	T	6	Q
S-1009C25I-N4T1U	T	6	R
S-1009C26I-N4T1U	T	6	S
S-1009C27I-N4T1U	T	6	T
S-1009C28I-N4T1U	T	6	U
S-1009C29I-N4T1U	T	6	V
S-1009C30I-N4T1U	T	6	W
S-1009C31I-N4T1U	T	6	X
S-1009C32I-N4T1U	T	6	Y
S-1009C33I-N4T1U	T	6	Z
S-1009C34I-N4T1U	T	7	A
S-1009C35I-N4T1U	T	7	B
S-1009C36I-N4T1U	T	7	C
S-1009C37I-N4T1U	T	7	D
S-1009C38I-N4T1U	T	7	E
S-1009C39I-N4T1U	T	7	F
S-1009C40I-N4T1U	T	7	G
S-1009C41I-N4T1U	T	7	H
S-1009C42I-N4T1U	T	7	I
S-1009C43I-N4T1U	T	7	J
S-1009C44I-N4T1U	T	7	K
S-1009C45I-N4T1U	T	7	L
S-1009C46I-N4T1U	T	7	M

3. SNT-4A



(1) to (3): Product code (refer to **Product name vs. Product code**)

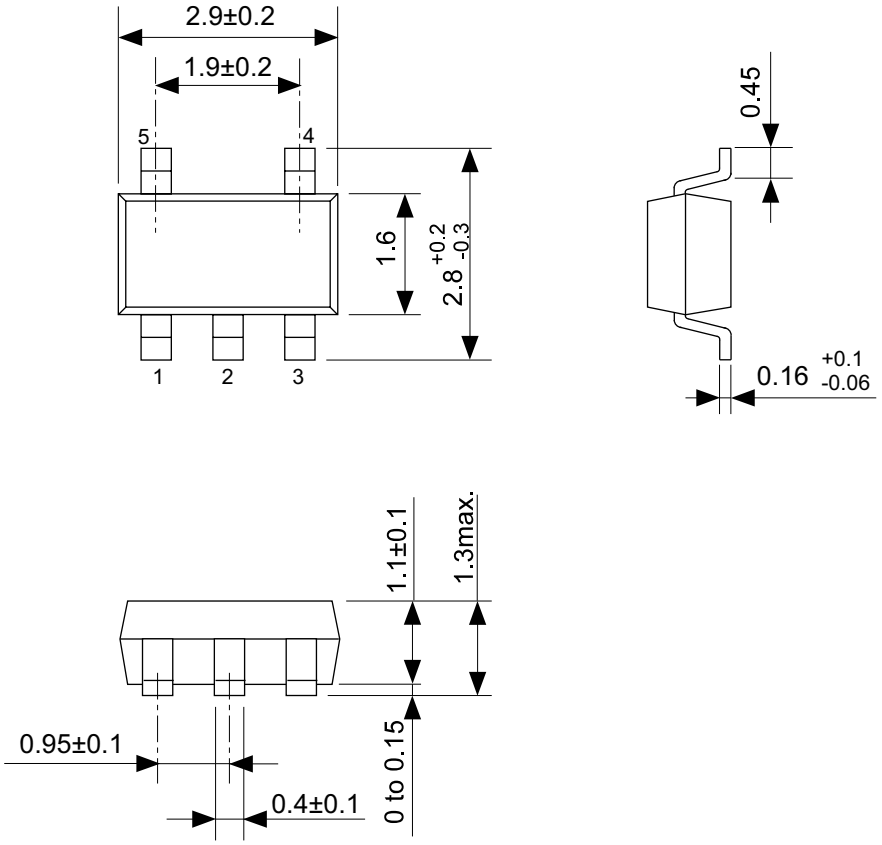
Product name vs. Product code

3. 1 Nch open-drain output product

Product Name	Product Code		
	(1)	(2)	(3)
S-1009N08I-I4T1U	T	8	A
S-1009N09I-I4T1U	T	8	B
S-1009N10I-I4T1U	T	8	C
S-1009N11I-I4T1U	T	8	D
S-1009N12I-I4T1U	T	8	E
S-1009N13I-I4T1U	T	8	F
S-1009N14I-I4T1U	T	8	G
S-1009N15I-I4T1U	T	8	H
S-1009N16I-I4T1U	T	8	I
S-1009N17I-I4T1U	T	8	J
S-1009N18I-I4T1U	T	8	K
S-1009N19I-I4T1U	T	8	L
S-1009N20I-I4T1U	T	8	M
S-1009N21I-I4T1U	T	8	N
S-1009N22I-I4T1U	T	8	O
S-1009N23I-I4T1U	T	8	P
S-1009N24I-I4T1U	T	8	Q
S-1009N25I-I4T1U	T	8	R
S-1009N26I-I4T1U	T	8	S
S-1009N27I-I4T1U	T	8	T
S-1009N28I-I4T1U	T	8	U
S-1009N29I-I4T1U	T	8	V
S-1009N30I-I4T1U	T	8	W
S-1009N31I-I4T1U	T	8	X
S-1009N32I-I4T1U	T	8	Y
S-1009N33I-I4T1U	T	8	Z
S-1009N34I-I4T1U	T	9	A
S-1009N35I-I4T1U	T	9	B
S-1009N36I-I4T1U	T	9	C
S-1009N37I-I4T1U	T	9	D
S-1009N38I-I4T1U	T	9	E
S-1009N39I-I4T1U	T	9	F
S-1009N40I-I4T1U	T	9	G
S-1009N41I-I4T1U	T	9	H
S-1009N42I-I4T1U	T	9	I
S-1009N43I-I4T1U	T	9	J
S-1009N44I-I4T1U	T	9	K
S-1009N45I-I4T1U	T	9	L
S-1009N46I-I4T1U	T	9	M

3. 2 CMOS output product

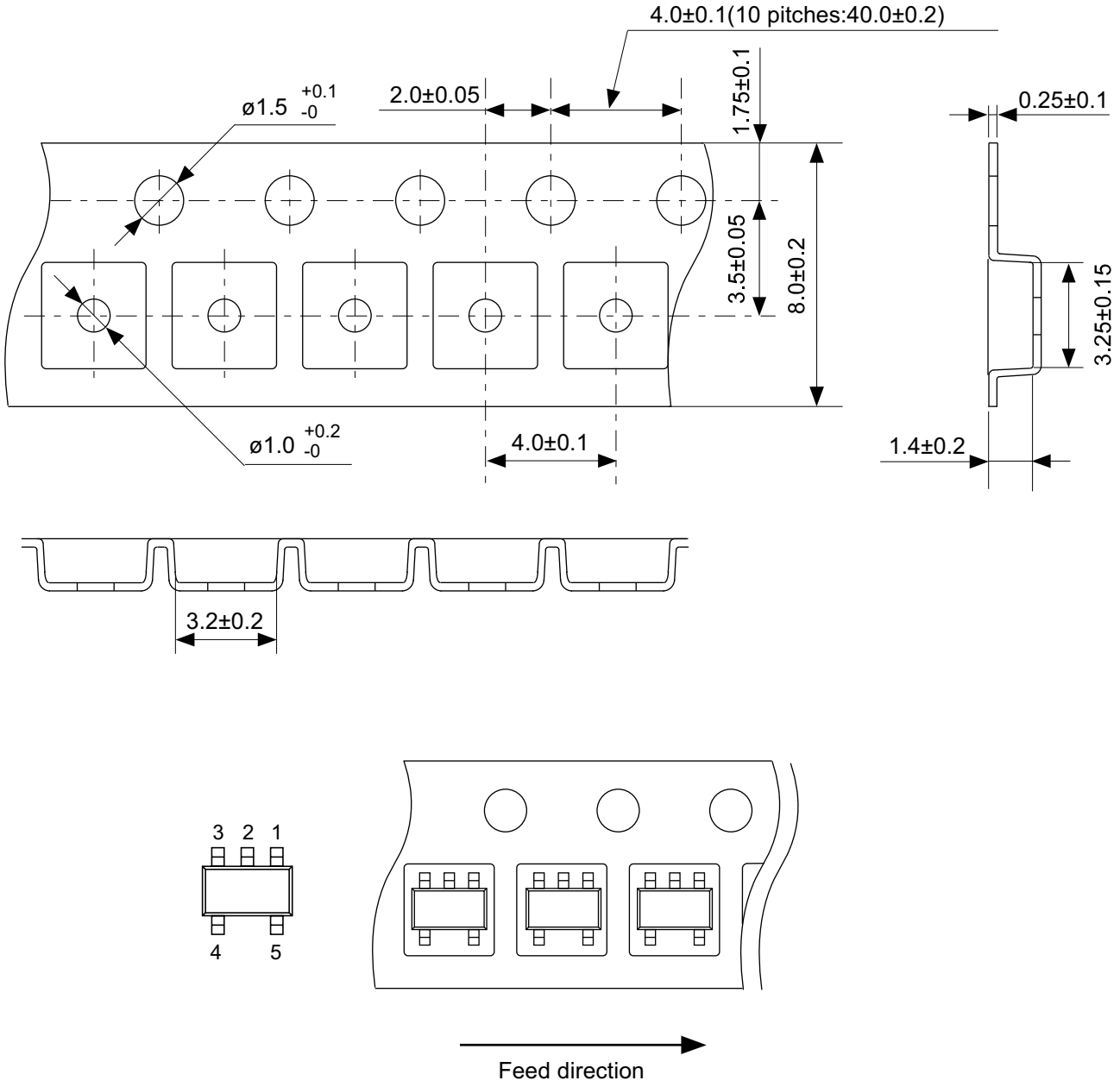
Product Name	Product Code		
	(1)	(2)	(3)
S-1009C08I-I4T1U	T	6	A
S-1009C09I-I4T1U	T	6	B
S-1009C10I-I4T1U	T	6	C
S-1009C11I-I4T1U	T	6	D
S-1009C12I-I4T1U	T	6	E
S-1009C13I-I4T1U	T	6	F
S-1009C14I-I4T1U	T	6	G
S-1009C15I-I4T1U	T	6	H
S-1009C16I-I4T1U	T	6	I
S-1009C17I-I4T1U	T	6	J
S-1009C18I-I4T1U	T	6	K
S-1009C19I-I4T1U	T	6	L
S-1009C20I-I4T1U	T	6	M
S-1009C21I-I4T1U	T	6	N
S-1009C22I-I4T1U	T	6	O
S-1009C23I-I4T1U	T	6	P
S-1009C24I-I4T1U	T	6	Q
S-1009C25I-I4T1U	T	6	R
S-1009C26I-I4T1U	T	6	S
S-1009C27I-I4T1U	T	6	T
S-1009C28I-I4T1U	T	6	U
S-1009C29I-I4T1U	T	6	V
S-1009C30I-I4T1U	T	6	W
S-1009C31I-I4T1U	T	6	X
S-1009C32I-I4T1U	T	6	Y
S-1009C33I-I4T1U	T	6	Z
S-1009C34I-I4T1U	T	7	A
S-1009C35I-I4T1U	T	7	B
S-1009C36I-I4T1U	T	7	C
S-1009C37I-I4T1U	T	7	D
S-1009C38I-I4T1U	T	7	E
S-1009C39I-I4T1U	T	7	F
S-1009C40I-I4T1U	T	7	G
S-1009C41I-I4T1U	T	7	H
S-1009C42I-I4T1U	T	7	I
S-1009C43I-I4T1U	T	7	J
S-1009C44I-I4T1U	T	7	K
S-1009C45I-I4T1U	T	7	L
S-1009C46I-I4T1U	T	7	M



No. MP005-A-P-SD-1.3

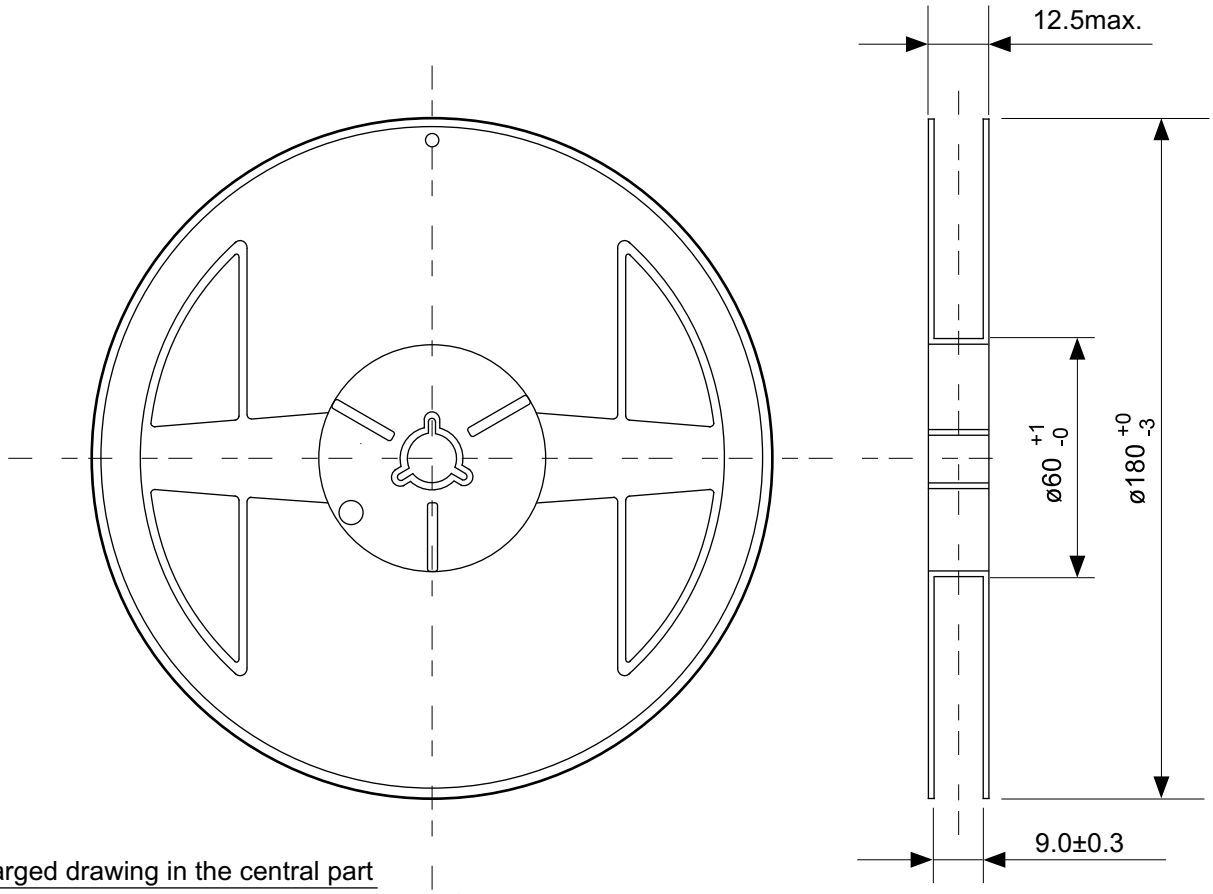
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

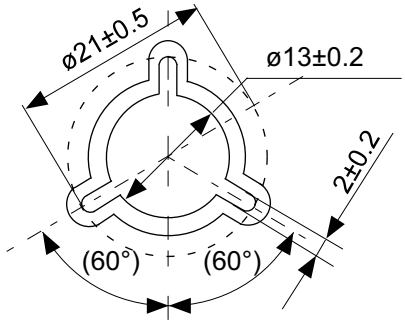


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

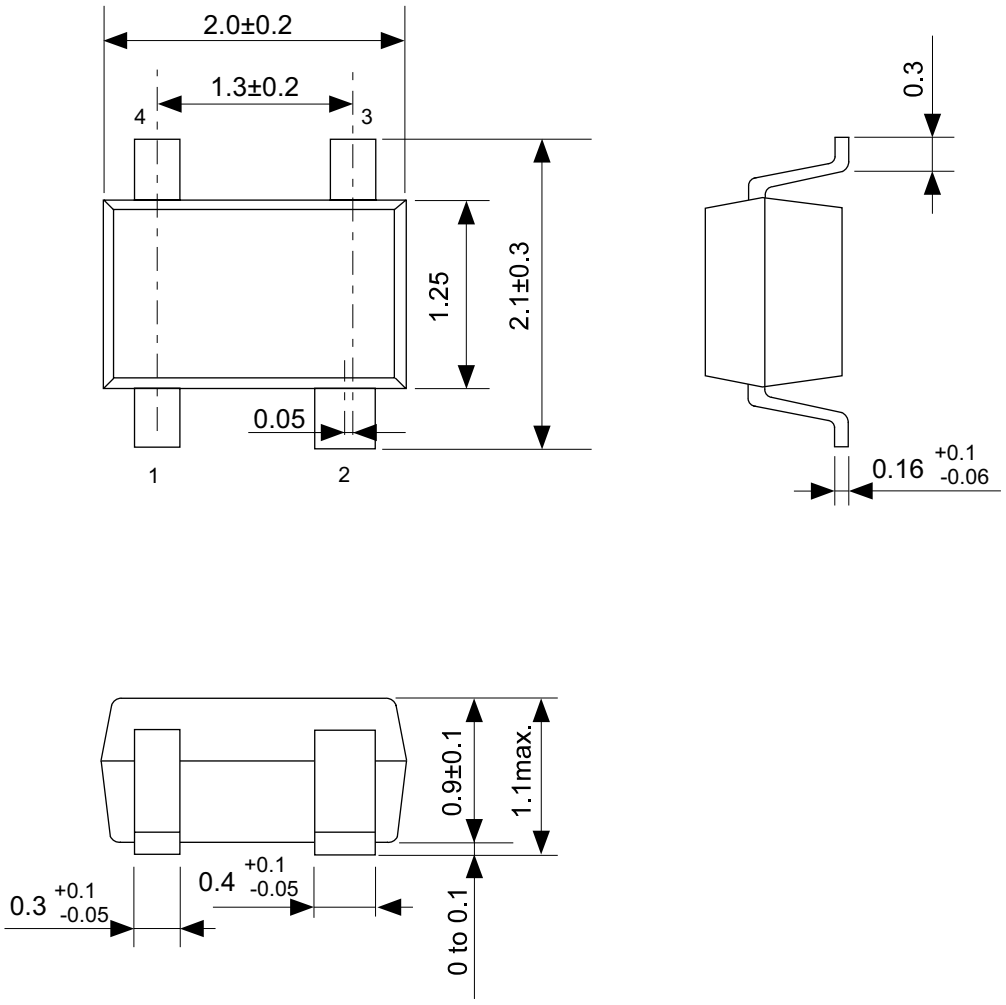


Enlarged drawing in the central part



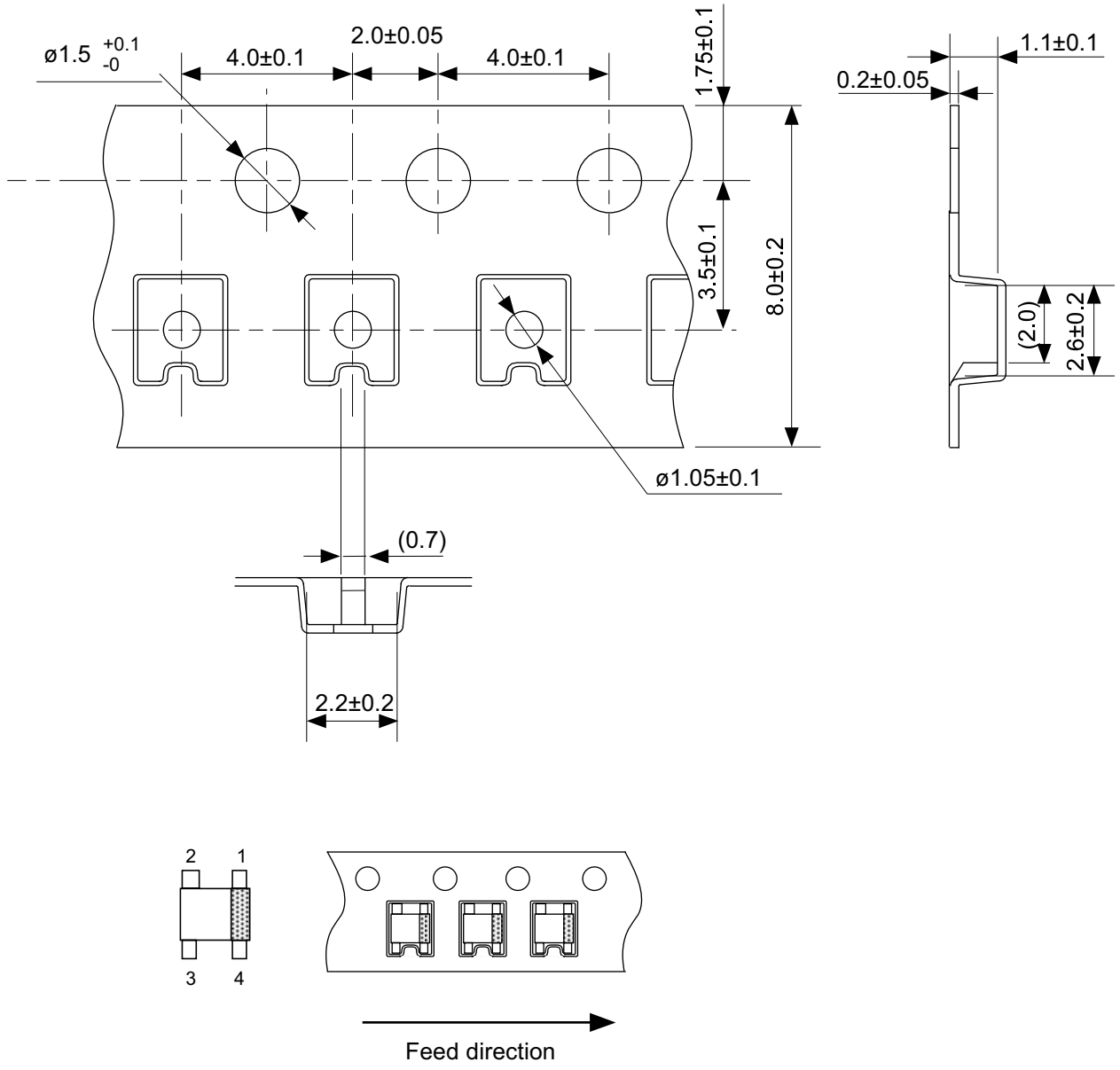
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



No. NP004-A-P-SD-2.0

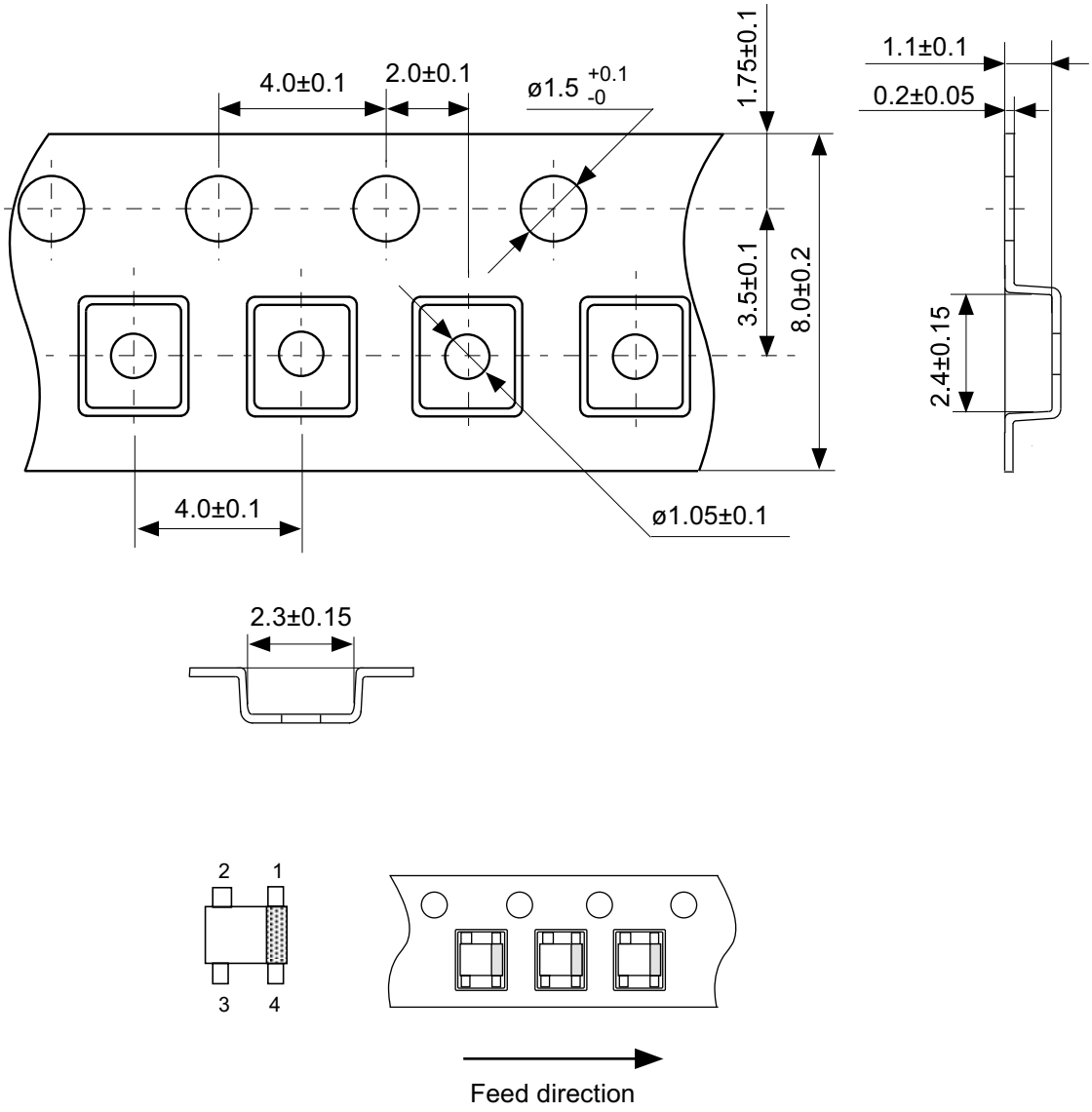
TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.



Feed direction

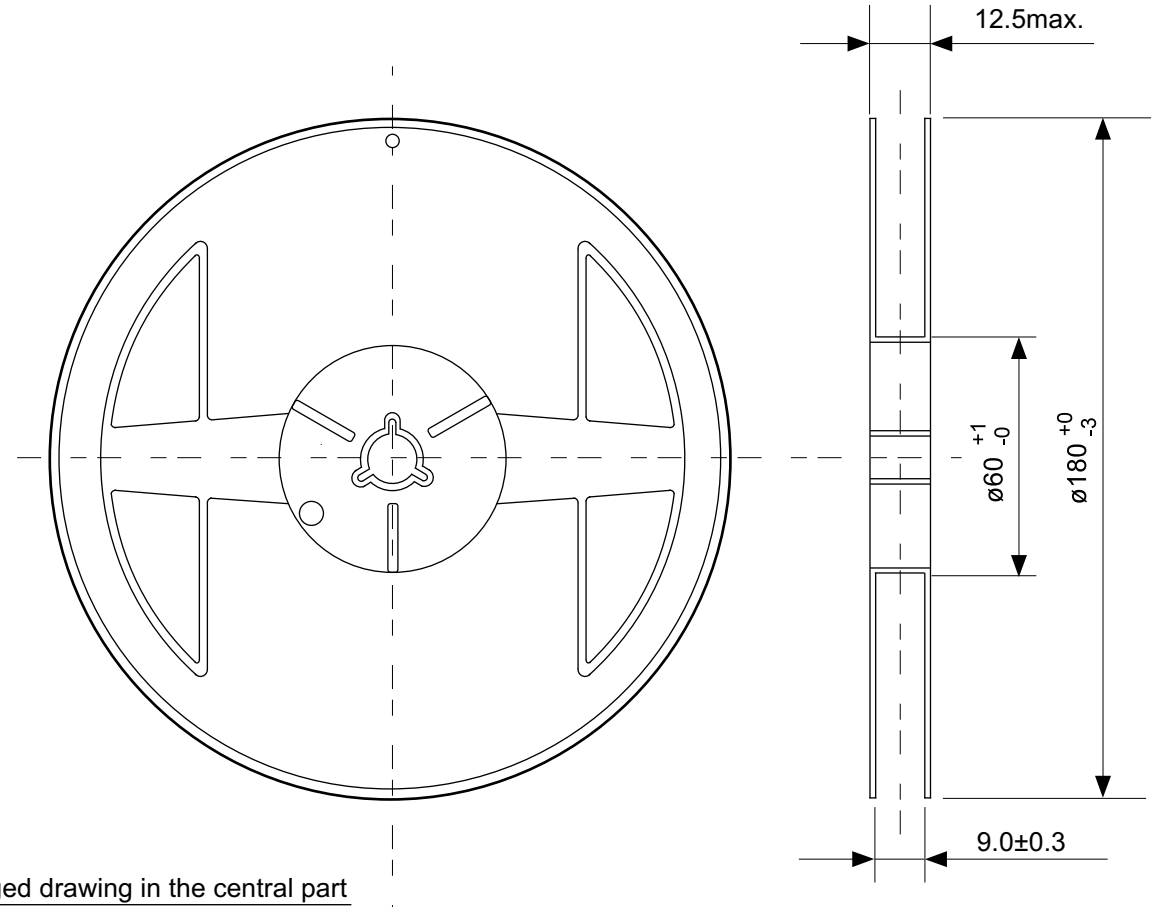
No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
ANGLE	
UNIT	mm
	ABLIC Inc.

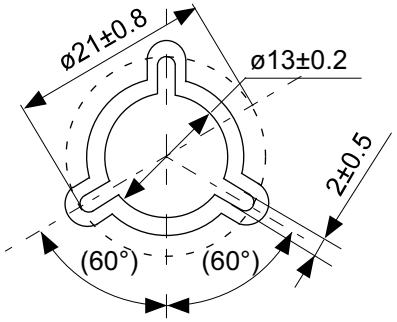


No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.

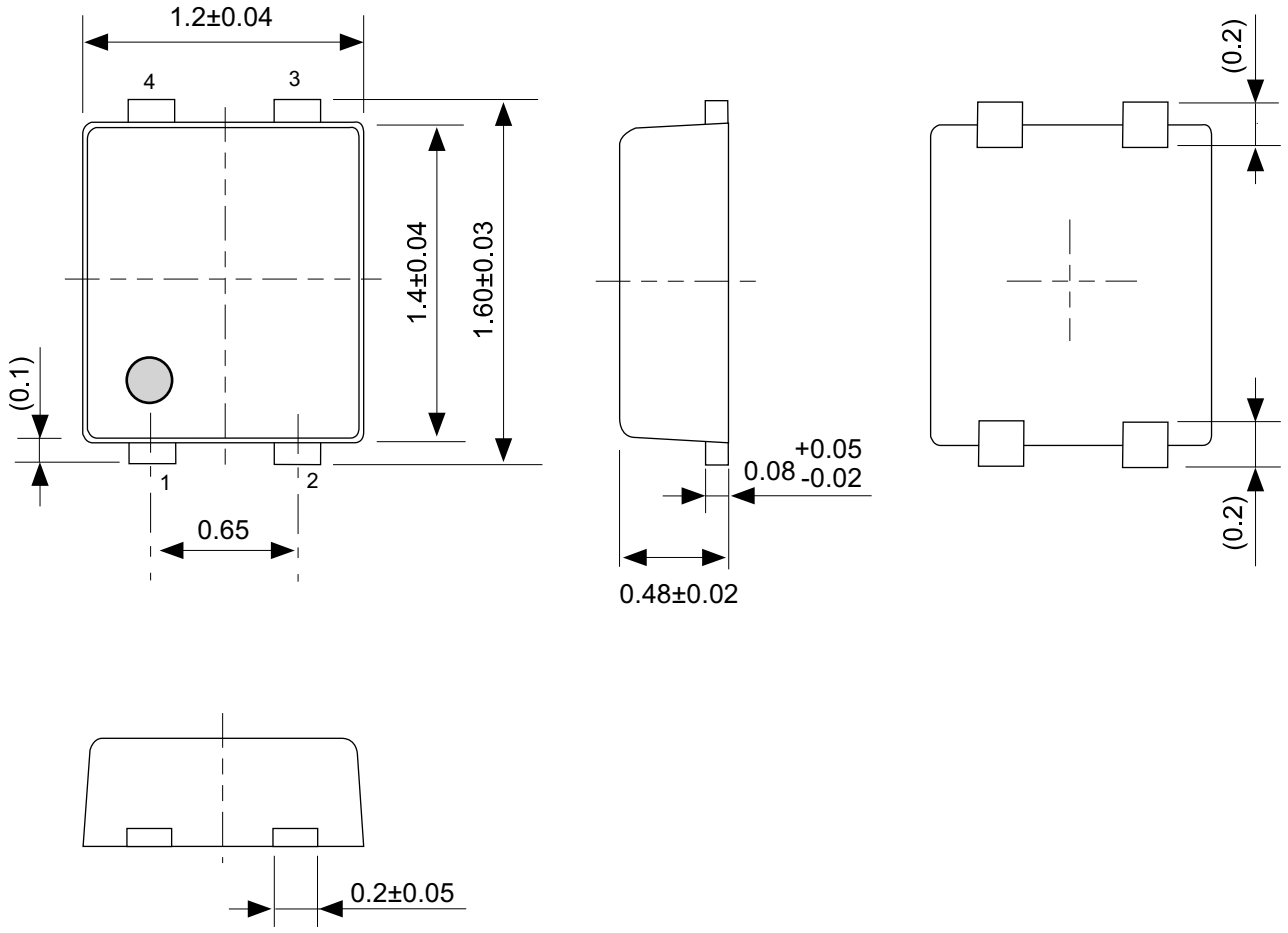


Enlarged drawing in the central part



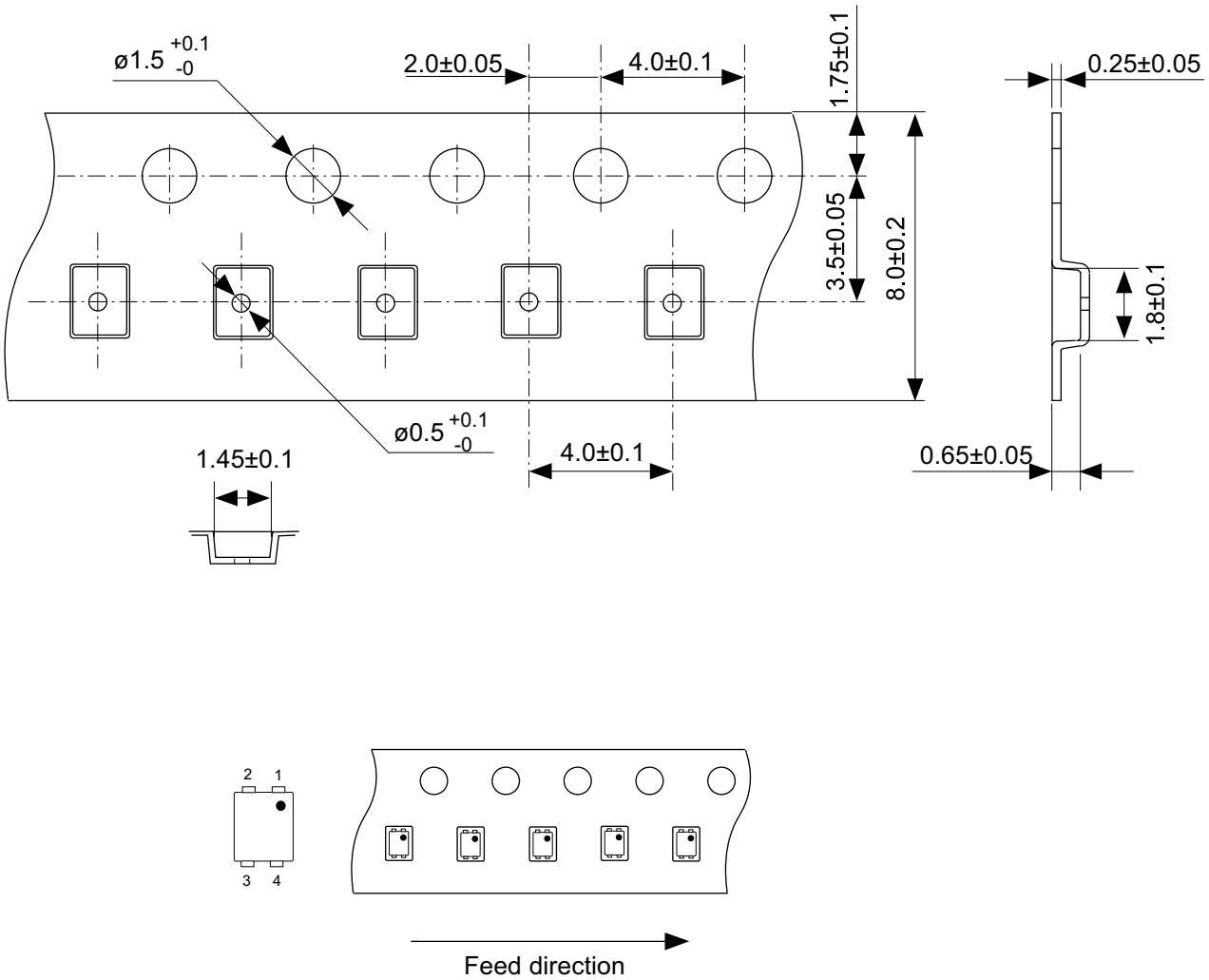
No. NP004-A-R-SD-1.1

TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		



No. PF004-A-P-SD-6.0

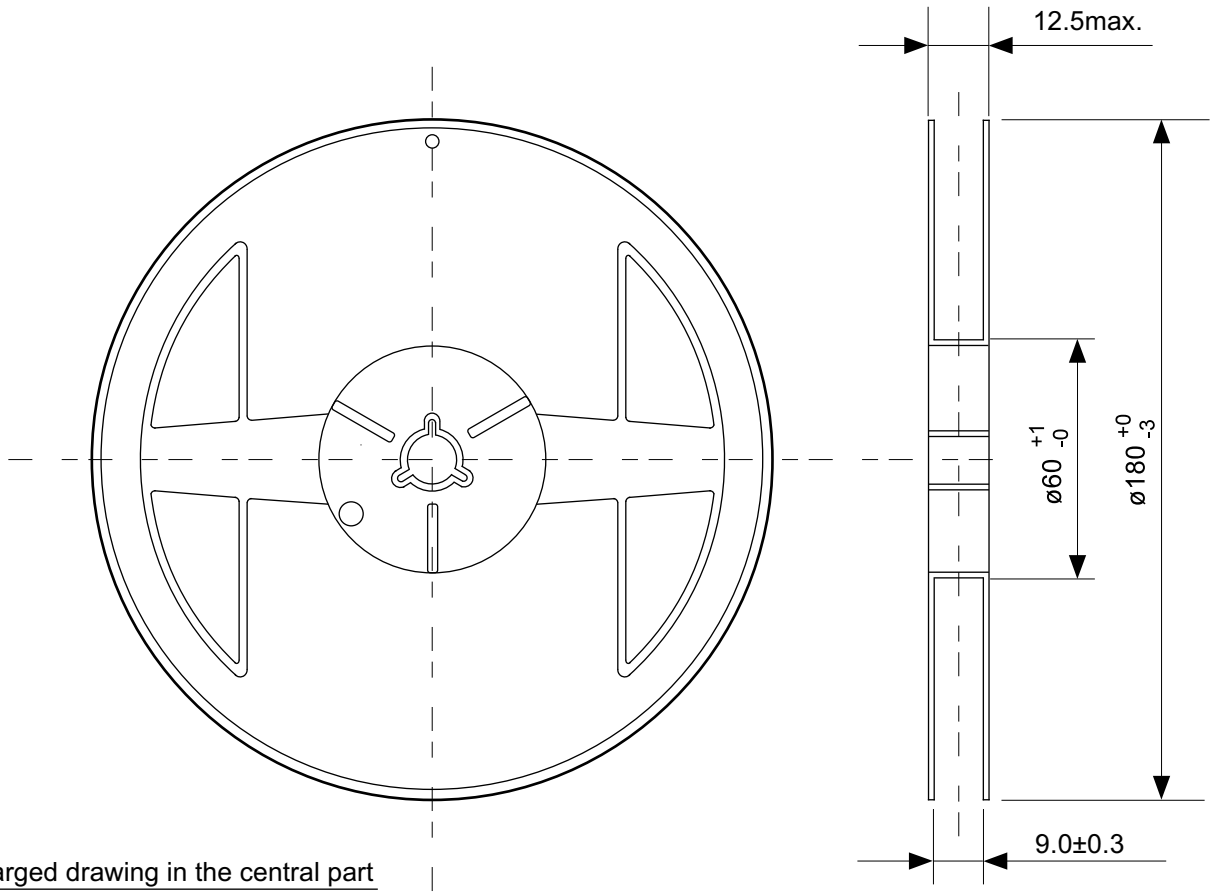
TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	



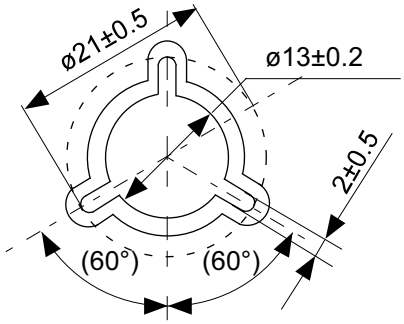
No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



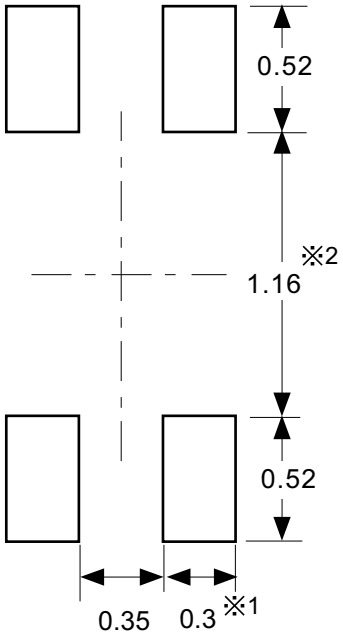
Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は ″SNTパッケージ活用の手引き″ を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not responsible for damages caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not responsible for damages caused by the incorrect information described herein.
4. Be careful to use the products within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not responsible for damages caused by failures and / or accidents, etc. that occur due to the use of the products outside their specified ranges.
5. When using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not apply the products to the above listed devices and equipments without prior written permission by ABLIC Inc.
   Especially, the products cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.
   Prior consultation with our sales office is required when considering the above uses.
   ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
   The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc.
    The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party without the express permission of ABLIC Inc. is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

2.2-2018.06