PCN Number:	20180202000	**PCN Date:**	Feb 9, 2018
Title:	Design Die Revision 3.1 Announcement for the 66AK2H06, 66AK2H12, 66AK2H14, and 66AK2HHP0		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	May 9, 2018	**Estimated Sample Availability:**	Date provided at sample request.

Change Type:					
☐	Assembly Site	☐	Assembly Process	☐	Assembly Materials
☒	Design	☒	Electrical Specification	☐	Mechanical Specification
☐	Test Site	☐	Packing/Shipping/Labeling	☐	Test Process
☐	Wafer Bump Site	☐	Wafer Bump Material	☐	Wafer Bump Process
☐	Wafer Fab Site	☐	Wafer Fab Materials	☐	Wafer Fab Process
		☒	Part number change		

PCN Details

Description of Change:

This notification is to inform of a Design Die Revision 3.1 for the 66AK2H06, 66AK2H12, 66AK2H14, and 66AK2HHP0 devices. Affected devices are listed in the Product Affected section of this document.

As part of this change, Design Die Revision 2.0 Part Numbers are being **replaced** by Design Die Revision 3.1 part numbers.

Change from Design Die Revision 2.0 to Design Die Revision 3.1 Summary:
Removed the following Data Sheet Errata Advisories:

- Advisory 34: Category=DDR3. DDR3 Limited to Highest Data Rates Due to Possibility of PLL Instability During Temperature Changes After Startup
- Advisory 35: Category=DDR3. Restrictions on DDR3 PLL Configuration and DDR3nCLK to Eliminate DDR3 Errors due to PLL Dynamic Phase Offset
- Advisory 36: Category=TeraNet. Two Masters Accessing Two C66x CorePac L2 Memories Can Cause TeraNet Hang
- Advisory 38: Category=PCI. PCI-Express Hot Reset Not Handled During Boot
- Advisory 40: Category=ROM. NAND Boot Failure When Booting Single Block Backup Images
- Advisory 41: Category=ROM. NAND Boot Failure With Bit Errors in ECC
- Advisory 42: Category=ROM. ARM Ethernet Boot Reinitializes the Switch with Reset Isolation Enabled, Which May Cause Lockup
- Advisory 46: Category=QMSS. Queue Diversion Failure
- Advisory 47: Category=ROM. SGMII, SRIO, Hyperlink, and PCIe boot may fail on some devices
- Usage Note 27: Category= 10GbE. Device Hang if 10GbE PCS Registers are Accessed After Performing a 10G Lane Reset

Technical details are available in the Product Datasheet Errata documents in the product folders available on http://ti.com or from your local sales representative.

66AK2H06, 66AK2H12, 66AK2H14

Reason for Change:

Design Die Revision

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

Positive. Specific Data Sheet Errata Advisories removed.

Changes to product identification resulting from this PCN:

Orderable Part number change.
The design revision changes in the Lot Trace Code line on the device topside marking.
See Data Sheet Errata referenced above or contact your local sales representative.

Product Affected:

Die Revision 2.0 Part Numbers Being Replaced	Die Revision 3.1 REPLACEMENT Part Numbers
66AK2H06BAAW2	66AK2H06DAAW2
66AK2H06BAAW24	66AK2H06DAAW24
66AK2H06BAAWA2	66AK2H06DAAWA2
66AK2H06BAAWA24	66AK2H06DAAWA24
66AK2H06BXAAW2	66AK2H06DXAAW2
66AK2H12BAAW2	66AK2H12DAAW2
66AK2H12BAAW24	66AK2H12DAAW24
66AK2H12BAAWA2	66AK2H12DAAWA2
66AK2H12BAAWA24	66AK2H12DAAWA24
66AK2H12BXAAW2	66AK2H12DXAAWA24
66AK2H14BAAW24	66AK2H14DAAW24
66AK2H14BAAWA24	66AK2H14DAAWA24
66AK2H14BXAAW24	66AK2H14DXAAWA24
66AK2HHP0BXAAW2	66AK2HHP0DXAAW2

Qualification Report

Qualification Report for Device Families 66AK2H*AAAW*
Approved April 26, 2017

Product Attributes

Die Attributes	Qual Device: 66AK2H*
Die Revision	All
Wafer Fab Site	TSMC15
Wafer Fab Process	C28.P
Package Attributes	
Assembly Site	AMKOR-K4 and TI-Philippines
Package Family	FC-BGA
Green Status	Pb-free & Green
Flammability Rating	UL 94 V-0

- Device is qualified to preconditioning to MSL-4

Qualification Results for Qualification Device 66AK2H*

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Result	Pass / Fail
UHAST	Unbiased HAST, 130C/85%RH	96 hrs	3 / 231 / 0	Pass
TC	Temp Cycle, -40 / 125C	850 Cycles	3 / 231 / 0	Pass
TC	Temp Cycle, -55 / 125C	700 Cycles	3 / 78 / 0	Pass
THB	Bias. Temp & Humidity, 85C/85%RH @ Vdd	1000 hrs	3 / 75 / 0	Pass
HTSL	Bake 150C	1000 hrs Bake	3 / 231 / 0	Pass
HTOL	HTOL, Tj=125C	1000 hrs	3 / 356 / 0	Pass
HBM	ESD - HBM	±1000V	1 / 3 / 0	Pass
CDM	ESD - CDM	±250V	1 / 3 / 0	Pass

LU	Latch-up, High Temp	±100 mA, 1.5 * Vmax @ 105C	1 / 3 / 0	Pass
BLR	0/100C BLR TC, IPC-9701	Cycles to fail / IPC-9701	Beta = 7.04, Eta = 5063, 1st Fail @ 3033 Cycles	Pass

Notes: Preconditioning to MSL-4 was performed for unbiased HAST, THB, Temperature Cycle, and storage bake.

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com